PRELIMINARY

Winbond Electronics Corp.

ISD1700 Series

Design Guide

October 2006 Revision 0

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1 GENERAL DESCRIPTION

The Winbond® ISD1700 ChipCorder® Series is a high quality, fully integrated, single-chip multi-message voice record and playback device ideally suited to a variety of electronic systems. The message duration is user selectable in ranges from 26 seconds to 120 seconds, depending on the specific device. The sampling frequency of each device can also be adjusted from 4 kHz to 12 kHz with an external resistor, giving the user greater flexibility in duration versus recording quality for each application. Operating voltage spans a range from 2.4 V to 5.5 V to ensure that the ISD1700 devices are optimized for a wide range of battery or line-powered applications.

The ISD1700 is designed for operation in either standalone or microcontroller (SPI) mode. The device incorporates a proprietary message management system that allows the chip to self-manage address locations for multiple messages. This unique feature provides sophisticated messaging flexibility in a simple push-button environment. The devices include an on-chip oscillator (with external resistor control), microphone preamplifier with Automatic Gain Control (AGC), an auxiliary analog input, anti-aliasing filter, Multi-Level Storage (MLS) array, smoothing filter, volume control, Pulse Width Modulation (PWM) Class D speaker driver, and current/voltage output.

The ISD1700 devices also support an optional “vAlert” (voiceAlert) feature that can be used as a new message indicator. With vAlert, the device flashes an external LED to indicate that a new message is present. Besides, four special sound effects are reserved for audio confirmation of operations, such as “Start Record”, “Stop Record”, “Erase”, “Forward”, “Global Erase”, and etc.

Recordings are stored into on-chip Flash memory, providing zero-power message storage. This unique single-chip solution is made possible through Winbond’s patented Multi-Level Storage (MLS) technology. Audio data are stored directly in solid-state memory without digital compression, providing superior quality voice and music reproduction.

Voice signals can be fed into the chip through two independent paths: a differential microphone input and a single-ended analog input. For outputs, the ISD1700 provides a Pulse Width Modulation (PWM) Class D speaker driver and a separate analog output simultaneously. The PWM can directly drive a standard 8Ω speaker or typical buzzer, while the separate analog output can be configured as a single-ended current or voltage output to drive an external amplifier.

While in Standalone mode, the ISD1700 devices automatically enter into power down mode for power conservation after an operation is completed.

In the SPI mode, the user has full control via the serial interface in operating the device. This includes random access to any location inside the memory array by specifying the start address and end address of operations. SPI mode also allows access to the Analog Path Configuration (APC) register. This register allows flexible configuration of audio paths, inputs, outputs and mixing. The APC default configuration for standalone mode can also be modified by storing the APC data into a non-volatile register (NVCFG) that is loaded at initialization. Utilizing the capabilities of ISD1700 Series, designers have the control and flexibility to implement voice functionality into the high-end products.

Notice: The specifications are subject to change without notice. Please contact Winbond Sales Offices or Representatives to verify current or future specifications. Also, refer to the website for any related application notes.

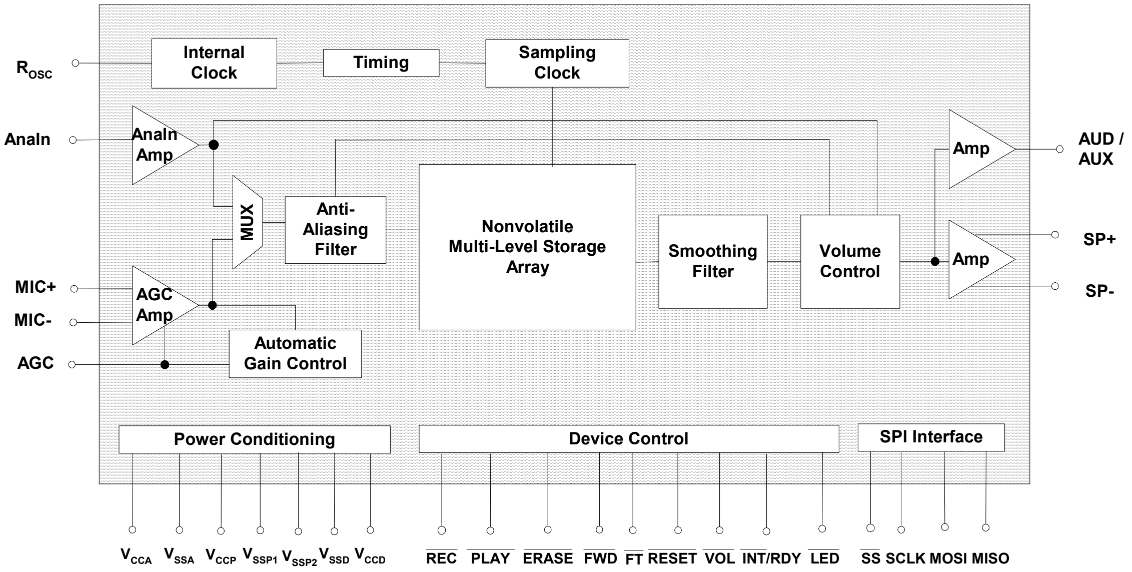
2 FEATURES

- Integrated message management systems for single-chip, push-button applications
  - $\overline{\textbf{REC}}$ *:* level-trigger for recording
  - $\overline{\textbf{PLAY}}$ *:* edge-trigger for individual message or level-trigger for looping playback sequentially
  - $\overline{\textbf{ERASE}}$ *:* edge-triggered erase for first or last message or level-triggered erase for all messages
  - $\overline{\textbf{FWD}}$ *:* edge-trigger to advance to the next message or fast message scan during the playback
  - $\overline{\textbf{VOL}}$: 8 levels output volume control
  - RDY/$\overline{\text{INT}}$: ready or busy status indication
  - $\overline{\textbf{RESET}}$: return to the default state
  - Automatic power-down after each operation cycle
- Selectable sampling frequency controlled by an external oscillator resistor

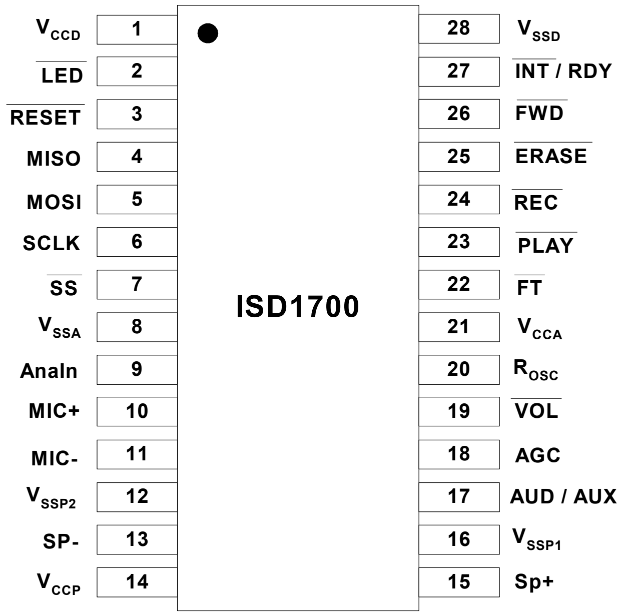
Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Rosc	60 kΩ	80 kΩ	100 kΩ	120 kΩ	160 kΩ

- Selectable message duration
  - A wide range selection from 30 secs to 240 secs at 8 kHz sampling frequency
- Message and operation indicators
  - Four customizable Sound Effects (SEs) for audible indication
  - Optional vAlert (voiceAlert) to indicate the presence of new messages
  - LED: stay on during recording, blink during playback, forward and erase operations
- Dual operating modes
  - *Standalone mode:*
    - Integrated message management techniques
    - Automatic power-down after each operation cycle
  - *SPI mode:*
    - Fully user selectable and controllable options via APC register and various SPI commands
- Two individual input channels
  - MIC+/MIC-: differential microphone inputs with AGC (Automatic Gain Control)
  - AnaIn: single-ended auxiliary analog input for recording or feed-through
- Dual output channels
  - Differential PWM Class D speaker outputs directly drives an 8 Ω speaker or a typical buzzer
  - Configurable AUD (current) or AUX (voltage) single-ended output drives external audio amplifier
- ChipCorder standard features
  - High-quality, natural voice and audio reproduction
  - 2.4V to 5.5V operating voltage
  - 100-year message retention (typical)
  - 100,000 record cycles (typical)
- Temperature options:
  - Commercial: 0°C to +50°C (die); 0°C to +70°C (packaged units)
  - Industrial: -40°C to +85°C (packaged units)
- Packaging types: available in die, PDIP, SOIC and TSOP
- Package option: Lead-free packaged units

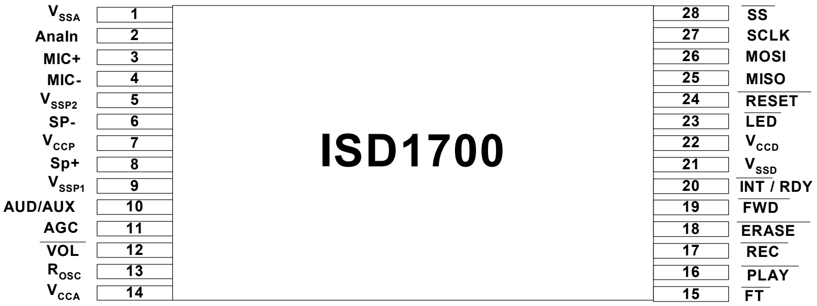
3 BLOCK DIAGRAM



4 PINOUT CONFIGURATION



SOIC / PDIP



TSOP

5 PIN DESCRIPTION

PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS [3]
V_{CCD}	1	22	**Digital Power Supply**: It is important to have a separate path for each power signal including V_{CCD}, V_{CCA} and V_{CCP} to minimize the noise coupling. Decoupling capacitors should be as close to the device as possible.
$\overline{\text{LED}}$	2	23	**LED**: With an LED connected, this output turns an LED on during recording and blinks LED during playback, forward and erase operations.
$\overline{\text{RESET}}$	3	24	**RESET**: When Low, the device enters into a known state and initializes all pointers to the default state. This pin has an internal pull-up resistor [1].
MISO	4	25	**Master In Slave Out:** Data is shifted out on the falling edge of SCLK. When the SPI is inactive ($\overline{\text{SS}}$ = high), it's tri-state.
MOSI	5	26	**Master Out Slave In:** Data input of the SPI interface when the device is configured as slave. Data is latched into the device on the rising edge of SCLK. This pin has an internal pull-up resistor [1].
SCLK	6	27	**Serial Clock:** Clock of the SPI interface. It is usually generated by the master device (typically microcontroller) and is used to synchronize the data transfer in and out of the device through the MOSI and MISO lines, respectively. This pin has an internal pull-up resistor [1].
$\overline{\text{SS}}$	7	28	**Slave Select:** This input, when low, selects the device as slave device and enables the SPI interface. This pin has an internal pull-up resistor [1].
V_{SSA}	8	1	**Analog Ground**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.
AnaIn	9	2	**AnaIn:** Auxiliary analog input to the device for recording or feed-through. An AC-coupling capacitor (typical 0.1uF) is necessary and the amplitude of the input signal must not exceed 1.0 Vpp. Depending upon the D3 of APC register, AnaIn signal can be directly recorded into the memory, mixed with the Mic signal then recorded into the memory or buffered to the speaker and AUD/AUX outputs via feed-through path.
MIC+	10	3	**MIC+:** Non-inverting input of the differential microphone signal. The input signal should be AC-coupled to this pin via a series capacitor. The capacitor value, together with an internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the pass band filter. The Mic analog path is also controlled by D4 of APC register.
MIC-	11	4	**MIC-**: Inverting input of the differential microphone signal. The input signal should be AC-coupled to the MIC+ pin. It provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device. The Mic analog path is also controlled by D4 of APC register.
V_{SSP2}	12	5	**Ground for Negative PWM Speaker Driver**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.

PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS [3]
SP-	13	6	**SP-**: The negative Class D PWM provides a differential output with SP+ pin to directly drive an 8 Ω speaker or typical buzzer. During power down or not used, this pin is tri-stated. This output can be controlled by D8 of APC register. The factory default is set at on state.
V_{CCP}	14	7	**Power Supply for PWM Speaker Driver**: It is important to have a separate path for each power signal including V_{CCD}, V_{CCA} and V_{CCP} to minimize the noise coupling. Decoupling capacitors to V_{SSP1} and V_{SSP2} should be as close to the device as possible. The V_{CCP} supply and V_{SSP} ground pins have large transient currents and need low impedance returns to the system supply and ground, respectively.
SP+	15	8	**SP+:** The positive Class D PWM provides a differential output with the SP- pin to directly drive an 8 Ω speaker or typical buzzer. During power down or not used, this pin is tri-stated. This output can be controlled by D8 of APC register. The factory default is set at on state.
V_{SSP1}	16	9	**Ground for Positive PWM Speaker Driver**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.
AUD / AUX	17	10	**Auxiliary Output**: Depending upon the D7 of APC register, this output is either an AUD or AUX output. AUD is a single-ended current output, whereas AUX is a single-ended voltage output. They can be used to drive an external amplifier. The factory default is set to AUD. This output can be powered down by D9 of APC register. The factory default is set to On state. For AUD output, there is a ramp up at beginning and ramp down at the end to reduce the pop.
AGC	18	11	**Automatic Gain Control (AGC)**: The AGC adjusts the gain of the preamplifier dynamically to compensate for the wide range of microphone input levels. The AGC allows the full range of signals to be recorded with minimal distortion. The AGC is designed to operate with a nominal capacitor of 4.7 µF connected to this pin. Connecting this pin to ground (V_{SSA}) provides maximum gain to the preamplifier circuitry. Conversely, connecting this pin to the power supply (V_{CCA}) provides minimum gain to the preamplifier circuitry.
$\overline{\text{VOL}}$	19	12	**Volume:** This control has 8 levels of volume adjustment. Each Low going pulse decreases the volume by one level. Repeated pulses decrease volume level from current setting to minimum then increase back to maximum, and continue this pattern. During power-up or $\overline{\text{RESET}}$, a default setting is loaded from non-volatile configuration. The factory default is set to maximum. This output can also be controlled by <D2:D0> of APC register. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end allowing the use of a push button switch.
R_{OSC}	20	13	**Oscillator Resistor**: A resistor connected from R_{OSC} pin to ground determines the sample frequency of the device, which sets the duration. Please refer to the Duration Section for details.

PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS [3]
V_{CCA}	21	14	**Analog Power Supply**. It is important to have a separate path for each power signal including V_{CCD}, V_{CCA} and V_{CCP} to minimize the noise coupling. Decoupling capacitors to V_{SSA} should be as close to the device as possible.
$\overline{\text{FT}}$	22	15	**Feed-through:** In Standalone mode, when FT is engaged low, the AnaIn feed-through path is activated. As a result, the AnaIn signal is transmitted directly from AnaIn to both Speaker and AUD/AUX outputs with Volume Control. However, SPI overrides this input, while in SPI mode, and feed-through path is controlled by a D6 of APC register. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end allowing the use of a push button switch.
$\overline{\text{PLAY}}$	23	16	**Playback:** Pulsing **$\overline{\text{PLAY}}$** to Low once initiates a playback operation. Playback stops automatically when it reaches the end of the message. Pulsing it to Low again during playback stops the operation. Holding **$\overline{\text{PLAY}}$** Low constantly functions as a sequential playback operation loop. This looping continues until **$\overline{\text{PLAY}}$** returns to High. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end allowing the use of a push button switch.
$\overline{\text{REC}}$	24	17	**Record:** The device starts recording whenever **$\overline{\text{REC}}$** switches from High to Low and stays at Low. Recording stops when the signal returns to High. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start allowing the use of a push button switch.
$\overline{\text{ERASE}}$	25	18	**Erase:** When active, it starts an erase operation. Erase operation will take place only when the playback pointer is positioned at either the first or last message. Pulsing this pin to Low enables erase operation and deletes the current message. Holding this pin Low for more than 3 sec. initiates a global erase operation, and will delete all the messages. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end allowing the use of a push button switch.
$\overline{\text{FWD}}$	26	19	**Forward:** When triggered, it advances to the next message from the current location, when the device is in power down status. During playback cycle, pulsing this pin Low stops the current playback operation and advances to the next message, and then re-starts the playback operation of the new message. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end allowing the use of a push button switch.
RDY/$\overline{\text{INT}}$	27	20	An open drain output. ***Ready (Standalone mode)**:* This pin stays Low during record, play, erase and forward operations and stays High in power down state ***Interrupt (SPI mode)**:* After completing the SPI command, an active low interrupt is generated. Once the interrupt is cleared, it returns to High.

PIN NAME	PDIP / SOIC	TSOP	FUNCTIONS [3]
V_{SSD}	28	21	**Digital Ground**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.

Note: [1] 600 kΩ

[2] TDeb = Refer to AC Timing

[3] For any unused pins, left floated.

6 FUNCTIONAL DESCRIPTION

6.1 DETAILED DESCRIPTION

6.1.1 Audio Quality

Winbond's patented ChipCorder® Multi-Level Storage (MLS) technology provides a natural, high-quality record and playback solution on a single chip. The input voice signals are stored directly in the Flash memory and are reproduced in their natural form without any of the compression artifacts caused by digital speech solutions.

6.1.2 Message Duration

The ISD1700 Series offer record and playback duration from 20 seconds to 480 seconds. Sampling frequency and message duration, T_{Dur}, are determined by an external resistor connected to the R_{OSC} pin.

Table 6.1 Duration vs. Sampling Frequency

Sample Freq.	ISD1730	ISD1740	ISD1750	ISD1760	ISD1790	ISD17120	ISD17150	ISD17180	ISD17210	ISD17240
12 kHz	20 secs	26 secs	33 secs	40 secs	60 secs	80 secs	100 secs	120 secs	140 secs	160 secs
8 kHz	30 secs	40 secs	50 secs	60 secs	90 secs	120 secs	150 secs	180 secs	210 secs	240 secs
6.4 kHz	37 secs	50 secs	62 secs	75 secs	112 secs	150 secs	187 secs	225 secs	262 secs	300 secs
5.3 kHz	45 secs	60 secs	75 secs	90 secs	135 secs	181 secs	226 secs	271 secs	317 secs	362 secs
4 kHz	60 secs	80 secs	100 secs	120 secs	180 secs	240 secs	300 secs	360 secs	420 secs	480 secs

6.1.3 Flash Storage

The ISD1700 devices utilize embedded Flash memory to provide non-volatile storage. A message can be retained for a minimum of 100 years without power. Additionally, each device can be re-recorded over 100,000 times (typical).

6.2 MEMORY ARRAY ARCHITECTURE

The memory array provides storage of four special Sound Effects (SEs) as well as the voice data. The memory array is addressed by rows. A row is the minimum storage resolution by which the memory can be addressed. The memory assignment is automatically handled by the internal message management system in standalone mode. While in SPI mode, one has the full access to the entire memory via the eleven address bits. Table 6.2 shows the minimum storage resolution with respect to the sampling frequency.

Table 6.2 Minimum Storage Resolution vs. Sampling Frequency

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Minimum Storage Resolution	83.3 msec	125 msec	156 msec	187 msec	250 msec

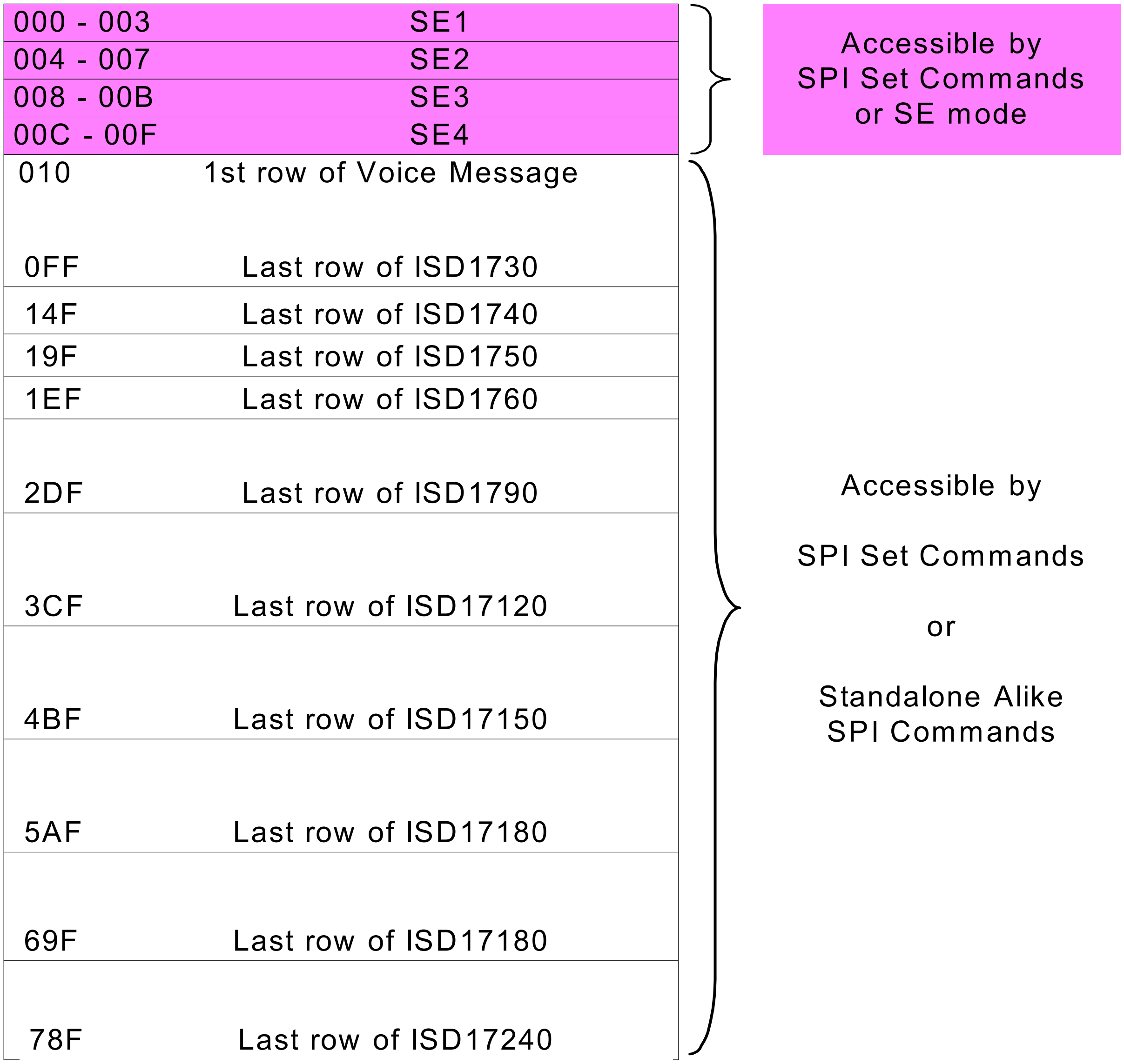
For example, at 8 kHz sampling frequency, the minimum storage resolution is 125 msec, so each Sound Effect (SE) is approximately 0.5 second long.

Table 6.3 shows the maximum row address of each device in the ISD1700 family. The four sound effects (SE) occupy the first sixteen rows in the memory array with four rows for each SE. That means from address 0x000 to address 0x00F. The remaining memory is dedicated to voice data storage. Hence, the address of voice message storage will start from 0x010 to the end of memory array.

Table 6.3 Device Maximum Row Address

Device	ISD1730	ISD1740	ISD1750	ISD1760	ISD1790	ISD17120	ISD17150	ISD17180	ISD17210	ISD17240
Maximum Address	0x0FF	0x14F	0x19F	0x1EF	0x2DF	0x3CF	0x4BF	0x5AF	0x69F	0x78F

Below figure shows the memory array architecture for ISD1700 series.



000 - 003	SE1
004 - 007	SE2
008 - 00B	SE3
00C - 00F	SE4
010	1st row of Voice Message
0FF	Last row of ISD1730
14F	Last row of ISD1740
19F	Last row of ISD1750
1EF	Last row of ISD1760
2DF	Last row of ISD1790
3CF	Last row of ISD17120
4BF	Last row of ISD17150
5AF	Last row of ISD17180
69F	Last row of ISD17180
78F	Last row of ISD17240

Accessible by
SPI Set Commands
or SE mode

Accessible by

SPI Set Commands

or

Standalone Alike
SPI Commands

6.3 Modes of Operations

The ISD1700 Series can operate in either Standalone (Push-Button) or microcontroller (SPI) mode.

6.3.1 Standalone (Push-Button) Mode

Standalone operation entails use of the $\overline{\textbf{REC}}$, $\overline{\textbf{PLAY}}$, $\overline{\textbf{FT}}$, $\overline{\textbf{FWD}}$, $\overline{\textbf{ERASE}}$, $\overline{\textbf{VOL}}$ and $\overline{\textbf{RESET}}$ pins to trigger operations. The internal state machine automatically configures the audio path according to the desired operation. In this mode, the internal state machine takes full control on message management. This allows the user to record, playback, erase, and forward messages without the needs to know the exact addresses of the messages stored inside the memory. For additional information, refer to Standalone Mode Design Reference Guide.

6.3.2 SPI Mode

In SPI mode, control of the device is achieved through the 4-wire serial interface. Commands similar to the push button controls, such as $\overline{\textbf{REC}}$, $\overline{\textbf{PLAY}}$, $\overline{\textbf{FT}}$, $\overline{\textbf{FWD}}$, $\overline{\textbf{ERASE}}$, $\overline{\textbf{VOL}}$ and $\overline{\textbf{RESET}}$, can be executed through the SPI interface. In addition, there are commands that allow the modification of the analog path configuration, as well as commands that direct access the memory address of the array, plus others. The SPI mode allows full control of the device and the ability to perform complex message management rather than conform to the circular memory architecture as push-button mode. Refer to SPI Mode sections for details.

In addition, it is suggested that both the microcontroller and the ISD1700 device have the same power supply level for design simplicity.

In either mode, it is strongly recommended that any unused pins, no matter input or output, must be left floated or unconnected. Otherwise, it will cause the device becoming malfunction.

7 ANALOG PATH CONFIGURATION (APC)

The analog path of the ISD1700 can be configured to accommodate a wide variety of signal path possibilities. This includes the source of recording signals, mixing of input signals, mixing the playback signal with an input signal to the outputs, feed-through signal to the outputs and which outputs being activated.

The active analog path configuration is determined by a combination of the internal state of the device, i.e. desired operation (record or playback), the status of the $\overline{\text{FT}}$ and the contents of the APC register. The APC register is initialized by the internal non-volatile configuration (NVCFG) bits upon power-on-reset or reset function. The APC register can be read and loaded using SPI commands.

The factory default of NVCFG bits, <D11:D0>, is 0100 0100 0000 = 0x440. This configures the device with recording through the MIC inputs, FT via AnaIn input, playback from MLS, SE editing feature enabled, maximum volume level, active PWM driver and AUD current outputs. One can use SPI commands to modify the APC register and store it permanently into the NVCFG bits.

7.1 APC REGISTER

Details of the APC register are shown in Table 7.1.

Table 7.1 APC Register

Bit	Name	Description			Default
D0	VOL0	Volume control bits <D2:D0>: These provide 8 steps of -4dB per step volume adjustment. Each bit changes the volume by one step, where 000 = maximum and 111 = minimum.			000 (maximum)
D1	VOL1				
D2	VOL2				
D3	Monitor_Input	Monitor input signal at outputs during recording.			0 = Monitor_input is Disabled
		D3 = 0	Disable input signal to outputs during record		
		D3 = 1	Enable input signal to outputs during record		
D4	Mix_Input	Combined with $\overline{\text{FT}}$ in standalone mode or SPI_FT bit (D6) in SPI mode, D4 controls the input selection for recording.			0 = Mix_Input is Off
		D4 = 0	$\overline{\text{FT}}$ / D6= 0	AnaIn REC	
			$\overline{\text{FT}}$ / D6= 1	Mic REC	
		D4 = 1	$\overline{\text{FT}}$ / D6= 0	(Mic + AnaIn) REC	
			$\overline{\text{FT}}$ / D6= 1	Mic REC	
D5	SE_Editing	Enable or disable editing of Sound Effect in Standalone mode: where 0 = Enable, 1 = Disable			0 = Enable SE_Editing

Bit	Name	Description	Default

D6	SPI_FT	For SPI mode only. Once SPI_PU command is sent, the $\overline{\text{FT}}$ is disabled and replaced by this control bit (D6) with the same functionality. After exiting SPI mode through the PD command, the $\overline{\text{FT}}$ resumes control of feed-through (FT) function.
		D6 = 0 — FT function in SPI mode is On
		D6 = 1 — FT function in SPI mode is Off
			1 = SPI_FT is Off

D7	Analog Output: AUD/AUX	Select AUD or AUX: 0 = AUD, 1 = AUX	0 = AUD
D8	PWM SPK	PWM Speaker +/- outputs: 0 = Enabled, 1 = Disabled	0 = PWM enabled
D9	PU Analog Output	PowerUp analog output: 0 = On, 1 = Off	0 = On
D10	vAlert	vAlert: 0 = On, 1 = Off.	1 = Off
D11	EOM Enable	EOM Enable for SetPlay operation: 0 = Off, 1 = On. When this bit is set to 1, SetPlay operation will stop at EOM location, rather than the End Address.	0 = Off

7.2 DEVICE ANALOG PATH CONFIGURATIONS

Table 7.2 demonstrates the possible analog path configurations with ISD1700. The device can be in power-down, power-up, recording, playback and/or feed-through state depending upon the operation requested by the push-buttons or related SPI commands. The active path in each of these states is determined by D3 and D4 of the APC register, as well as either D6 of the APC register in SPI mode or the $\overline{\text{FT}}$ status in standalone mode. In addition,.D7~D9 of the APC register determine which output drivers are activated.

Table 7.2 Operational Paths

APC Register			Operational Paths		
D6/ $\overline{\text{FT}}$	D4 Mix	D3 Mon	Idle	Record	Playback
0	0	0	AnaIn FT	AnaIn Rec	(AnaIn + MLS) --> o/p
0	0	1	AnaIn FT	AnaIn Rec + AnaIn FT	(AnaIn + MLS) --> o/p
0	1	0	(Mic + AnaIn) FT	(Mic + AnaIn) Rec	(AnaIn + MLS) --> o/p
0	1	1	(Mic + AnaIn) FT	(Mic + AnaIn) Rec + (Mic + AnaIn) FT	(AnaIn + MLS) --> o/p
1	0	0	FT Disable	Mic Rec	MLS --> o/p
1	0	1	FT disable	Mic Rec + Mic FT	MLS --> o/p
1	1	0	FT disable	Mic Rec	MLS --> o/p
1	1	1	FT disable	Mic Rec + Mic FT	MLS --> o/p

8 STANDALONE (PUSH-BUTTON) OPERATIONS

One can utilize the $\overline{\textbf{REC}}$, $\overline{\textbf{PLAY}}$, $\overline{\textbf{FT}}$, $\overline{\textbf{FWD}}$, $\overline{\textbf{ERASE}}$, $\overline{\textbf{VOL}}$ or $\overline{\textbf{RESET}}$ control to initiate a desired operation. As completed, the device automatically enters into the power-down state. An unique message management system is executed under this mode, which links to an optional special Sound Effect (SE) feature to review certain operating status of the device. Hence, it is benefit to understand how SE functions first.

8.1 SOUND EFFECT (SE) MODE

SE mode can be manipulated by several control pins as described below. There are four special sound effects (SE1, SE2, SE3, and SE4). Audio clips can be programmed into the SEs as various indications. Each SE occupies four designated memory rows and the first sixteen memory rows are reserved for these four SEs evenly and sequentially.

8.1.1 Sound Effect (SE) Features

The functions of SEs are used to indicate the status of the following operations:

- SE1: Beginning of recording, forward or global erase warning
- SE2: End of recording, single erase or forward from last message
- SE3: Invalid erase operation
- SE4: Successful global erase

In general, the LED flashes once for SE1, twice for SE2, and so forth. It is crucial to recognize that the LED flashes accordingly regardless the SEs are programmed or not. When none of them is programmed, the blinking periods of SE1, SE2, SE3 and SE4 are defined as T_{LS1}, T_{LS2}, T_{LS3} and T_{LS4}, respectively. Once they are programmed, during operation, the device flashes LED and plays the related SE simultaneously. Nevertheless, the period of blinking LED, under this condition, is limited by the duration of the recorded SE. In addition, they are defined as T_{SE1}, T_{SE2}, T_{SE3} and T_{SE4}, respectively. These timing parameters also apply to the conditions elaborated in the following related sections. (Refer to AC timing parameter for details.)

8.1.2 Entering SE Mode

- First press and hold $\overline{\textbf{FWD}}$ Low for 3 seconds or more roughly. This action on $\overline{\textbf{FWD}}$ will usually blink LED once (and play SE1 simultaneously if SE1 is recorded). However, if playback pointer is at the last message or memory is empty, the chip will blink the LED twice (and play SE2 simultaneously if SE2 is recorded).
- While holding $\overline{\textbf{FWD}}$ Low, press and hold the $\overline{\textbf{REC}}$ Low until the LED blinks once.
- The LED flashing once again indicates that the device is now in SE mode. Once entering into SE mode, the SE1 is always the first one to be accessible.

8.1.3 SE Editing

- After into SE editing mode, one can perform record, play, or erase operation on each SE by pressing the appropriate buttons. For example, to record SE, simply press and hold

$\overline{\textbf{REC}}$. Similarly for play or erase function, pulse $\overline{\textbf{PLAY}}$ or $\overline{\textbf{ERASE}}$, respectively. Record source can be either Mic+/- or AnaIn.

- A subsequent $\overline{\textbf{FWD}}$ operation moves the record and playback pointers to the next SE sequentially. The LED will also blink one to four times after such operation to indicate which SE is active. If $\overline{\textbf{FWD}}$ is pressed while in SE4, the LED will flash once to indicate that SE1 is again active.
- While the LED is blinking, the device will ignore any input commands. One must wait patiently until the LED stops blinking completely before any record, play, erase or forward input should be sent.

8.1.4 Exiting SE Mode

- The required steps are the same as Entering SE mode. First press and hold $\overline{\textbf{FWD}}$ until the LED stops blinking (and related SE is played if SEs are programmed). Then, simultaneously press and hold the $\overline{\textbf{REC}}$ Low until the LED blinks twice (and device will play SE2 if SE2 is programmed). The device now exits the SE editing mode.

8.1.5 Sound Effect Duration

The duration of SEs is determined by the sampling frequency selected and illustrated in below table.

Table 8.1 Sound Effect Duration vs. Sampling Frequency

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Duration of SE	0.33 sec	0.5 sec	0.625 sec	0.75 sec	1 sec

8.2 OPERATION OVERVIEW

After power is applied or power-on-reset (POR), the device is in the factory default state and two internal record and playback pointers are initialized. (These two pointers are discussed later.) Then the active analog path is determined by the state of the $\overline{\textbf{FT}}$, the status of the APC register and the desired operation.

Up to four optional sound effects (SE1~SE4) can be programmed into the device to provide audible feedback to alert the user about the operating status. Simultaneously, the LED output provides visual indication about the operating status. During the active state of LED output, no new command will be accepted.

An unique message management technique is implemented. Under this mode, the recorded messages are stored sequentially into the embedded memory from the beginning to the end in a circular fashion automatically.

Two internal pointers, the record pointer and playback pointer, determine the location where an operation starts. After POR, these pointers are initialized as follows:

- If no messages are present, both point to the beginning of memory.

- If messages are present, the record pointer points to the next available memory row following the last message and the playback pointer points to the beginning of the last recorded message.

The playback pointer is affected either by the $\overline{\textbf{FWD}}$ or $\overline{\textbf{REC}}$ operation. The record pointer is updated to the next available memory row after each $\overline{\textbf{REC}}$ operation.

8.2.1 Record Operation

The $\overline{\textbf{REC}}$ controls recording operation. Once setting this pin Low, the device starts recording from the next available row in memory and continues recording until either the $\overline{\textbf{REC}}$ returns to High or the memory is full. The source of recording is from either MIC+/- or AnaIn, whereas the active analog configuration path is determined by the desired operation and the state of the $\overline{\textbf{FT}}$. The $\overline{\textbf{REC}}$ is debounced internally. After recording, the record pointer will move to the next available row from the last recorded message and the playback pointer will position at the beginning of the newly recorded message.

However, it is important to perform an Erase operation on the desired location before any recording proceeds. In addition, the power supply must remain On during the entire recording process. If power is interrupted during recording process, the circular memory architecture will be destroyed. As a result, next time when a push button operation starts, the LED will blink seven times, which indicates that something unusual has occurred, and the device will fail to perform the requested operation. Under such scenario, the only way to recover the chip to a proper state is to perform a Global Erase operation.

Message recording indicators:

The built-in message management technique associates special Sound Effects, SE1 and SE2, within the recording process.

a) When $\overline{\textbf{REC}}$ goes Low:

- If SE1 is not programmed, then the LED turns On immediately to indicate that a recording is in progress.
- If SE1 is programmed, device plays SE1 and blinks LED simultaneously. Then LED turns On to show recording is in process. The LED blinking period of SE1 is determined by the recorded duration of SE1 (T_{SE1}). (Refer to AC timing parameter and timing diagrams for details.)

b) When $\overline{\textbf{REC}}$ goes High or when the memory is full:

- If SE2 is not programmed, then the LED turns Off immediately to indicate that the recording halts.
- If SE2 is programmed, device plays SE2 and flashes LED simultaneously. Then LED turns Off to show recording stops. The LED blinking period of SE2 is determined by the recorded duration of SE2 (T_{SE2}).

Triggering of $\overline{\textbf{REC}}$ during a play, erase or forward operation is an illegal operation and will be ignored.

8.2.2 Playback Operation

Two playback modes can be executed by $\overline{\textbf{PLAY}}$, which is internally debounced.

a) ***Edge-trigger mode***: Pulsing $\overline{\textbf{PLAY}}$ Low once initiates a playback operation of the current message. Playback automatically stops at the end of the message. Pulsing $\overline{\textbf{PLAY}}$ again will re-play the message. During playback, the LED flashes and goes Off when the playback completes. Pulsing $\overline{\textbf{PLAY}}$ to Low again during playback stops the playback operation. Under these circumstances, the playback pointer remains at the start of the played message after the operation is completed.

b) ***Looping Playback mode***: As $\overline{\textbf{PLAY}}$ is held Low constantly, the device plays all messages sequentially from the current message to its previous message and loops the playback action. During the entire playback process, the LED flashes non-stop. Meanwhile, the looping playback mechanism is implemented in the following sequence: start playback from current message; as playback is over, perform a forward operation; start playback of new message; once playback completes, perform another forward action; start playback of new message, …..and so on. This looping pattern continues until $\overline{\textbf{PLAY}}$ is released. As $\overline{\textbf{PLAY}}$ is released, device will continue to playback the current message until completion. When playback stops, the playback pointer is set at the start of the halted message.

   If no SE1 and SE2 are programmed, after playing a message, except the last one, device flashes LED once with blinking period T_{LS1} due to forward action. As after the last message, device flashes LED twice with blinking period T_{LS2}.

   If both SE1 and SE2 are programmed, after playing a message, except the last one, device plays SE1 and flashes LED simultaneously due to forward action. Then device keeps on the playback of new message. Alternatively, after playing the last message, device plays SE2 and flashes LED simultaneously due to forward action. Then device maintains the playback of the first message. The LED blinking period of SE1 and SE2 are determined by the recorded durations of SE1 and SE2, respectively.

Triggering $\overline{\textbf{PLAY}}$ during a record, erase, or forward operation is an illegal operation and will be ignored.

8.2.3 Forward Operation

The $\overline{\textbf{FWD}}$ allows the device to advance the playback pointer to the next message in a forward direction. When the pointer reaches the last message, it will jump back to the first message. Hence, the movement is alike a circular fashion among the messages. The $\overline{\textbf{FWD}}$ is debounced internally. The effect of a Low-going pulse on the $\overline{\textbf{FWD}}$ depends on the current state of the device:

a) If the device is in power-down state and the playback pointer does not point to the last message, then:

   - The playback pointer will advance to the next message.
   - If SE1 is not recorded, device will flash LED once with blinking period T_{LS1}.
   - However, if SE1 is recorded, device plays SE1 and blinks the LED once simultaneously. The LED blinking period is determined by the recorded duration, T_{SE1}, of SE1.

b) If the device is in power-down state and the playback pointer points to the last message, then:

   - The playback pointer will advance to the first message.
   - If SE2 is not recorded, device will flash LED twice with blinking period T_{LS2}.
   - However, if SE2 is recorded, device plays SE2 and blinks the LED twice simultaneously. The LED blinking period is determined by the recorded duration, T_{SE2}, of SE2.

c) If the device is currently playing a message that is not the last one, then the device:

   - Halts the playback operation.
   - Advances the playback pointer to the next message.
   - If SE1 is not recorded, device will flash LED once with blinking period T_{LS1}.
   - However, if SE1 is recorded, device plays SE1 and blinks the LED once simultaneously. The LED blinking period is determined by the recorded duration, T_{SE1}, of SE1.
   - Playback the new message.
   - The LED flashes during this entire process.

d) If the device is currently playing the last message, then the device:

   - Halts the playback operation.
   - Advances the playback pointer to the first message.
   - If SE2 is not recorded, device will flash LED twice with blinking period T_{LS2}.
   - However, if SE2 is recorded, device simultaneously plays SE2 and blinks the LED twice. The LED blinking period is determined by the recorded duration, T_{SE2}, of SE2.
   - Playback the first message.
   - The LED flashes during this entire process.

Triggering of the $\overline{\textbf{FWD}}$ operation during an erase or record operation is an illegal operation and will be ignored.

8.2.4 Erase Operation

Erasing individual message takes place only if the playback pointer is at either the first or the last message. Erasing individual messages other than the first or last message is not permitted in standalone mode. However, global erase can be executed at any message location and will erase all messages, once completed successfully. The $\overline{\textbf{ERASE}}$ is debounced internally. These two erase modes are described as follows:

a) ***Individual Erase***: Only the first or last messages can be individually erased. Pulsing $\overline{\textbf{ERASE}}$ Low enables device responses differently pending upon the status of the device and the current location of the playback pointer:

   - If the device is in power down mode and the playback pointer currently points to the first (or last) message, then the device will:

   - Erase first (or last) message and flash LED twice with blinking period T_{LS2}, if SE2 is not programmed.
   - If SE2 is programmed, simultaneously play SE2 and flash the LED twice. The LED blinking period is determined by the recorded duration, T_{SE2}, of SE2.
   - Update the playback pointer to the new first message - previously the second message (or new last message - originally the second to the last message).
- If the device is in power down mode and the playback pointer is at any message other than the first or last message, then the device will:
   - Not erase any message and flash LED three times with blinking period T_{LS3}, if SE3 is not programmed.
   - If SE3 is programmed, simultaneously play SE3 and flash the LED three times. The LED blinking period is determined by the recorded duration, T_{SE3}, of SE3.
   - Not change to the playback pointer.
- If the device is currently playing the first (or last) message,
   - Stops the playback operation.
   - Erases the message as scenario one of individual erase mentioned earlier.
- If the device is currently playing any message other than the first or last message, then the device will:
   - Stops the playback operation.
   - Behave like scenario two of individual erase mentioned above.

b) ***Global Erase***: Level-triggering $\overline{\textbf{ERASE}}$ at Low for more than 2.5 seconds and holding it continuously will initiate the Global Erase operation and deletes all messages, except the Sound Effects (SEs). See the below figure for operation details. The device reacts differently according to the current condition of the device.

- If SEs are not programmed
   - The device will blink LED twice with blinking period T_{LS2} once $\overline{\textbf{ERASE}}$ is triggered to indicate the current message being erased if it is either the first or last one.
   - Or if current message is neither the first nor last one, LED will blink three times with blinking period T_{LS3} to show that current message is not erased.
   - If $\overline{\textbf{ERASE}}$ is kept Low constantly, the LED will be blinked seven times to indicate all messages being erased. However, if $\overline{\textbf{ERASE}}$ is released before the first three blinks of LED, then global erase operation will be abandoned. Otherwise, the global erase operation will be performed. The estimated total period of blinking seven times is defined as ($3^*T_{LS1} + T_{LS4}$).
- If SEs are programmed,
   - The device will play SE2 and flash the LED twice simultaneously once $\overline{\textbf{ERASE}}$ is triggered to indicate the current message being erased if it is either the first or last one.
   - Or if current message is neither the first nor last one, the device will play SE3 and flash the LED three times simultaneously to indicate that current message is not erased.

- After $\overline{\textbf{ERASE}}$ continues to be held Low for 2.5 seconds or more, the device plays SE1 three times with LED flashing simultaneously. This serves as a warning signal that after playing SE1 three times, then global erase will be performed. However, if $\overline{\textbf{ERASE}}$ is released before the playback of the third SE1, then global erase operation will be abandoned.
- As $\overline{\textbf{ERASE}}$ is maintained Low continuously, the device will erase all messages and play SE4 with LED flashing simultaneously upon completion.
- During this process, the blinking periods of twice, three times and four times are limited by the recorded durations of SE2, SE3 and SE4 (T_{SE2},T_{SE3} and T_{SE4}) respectively.

However, it is vital to maintain the power supply On during the erase process. If power is interrupted during such process, the circular memory architecture will be destroyed. As a result, next time when a push button operation starts, the LED will blink seven times, which indicates that something abnormal has occurred, and the device will fail to perform the requested operation. Under such scenario, the only way to recover the chip to a proper state is to perform a Global Erase operation.

Triggering $\overline{\textbf{ERASE}}$ for individual erase during a record or forward operation is an illegal operation and will be ignored. However, triggering $\overline{\textbf{ERASE}}$ for an individual erase operation during playback will delete the current played message, if it is the first or last one.

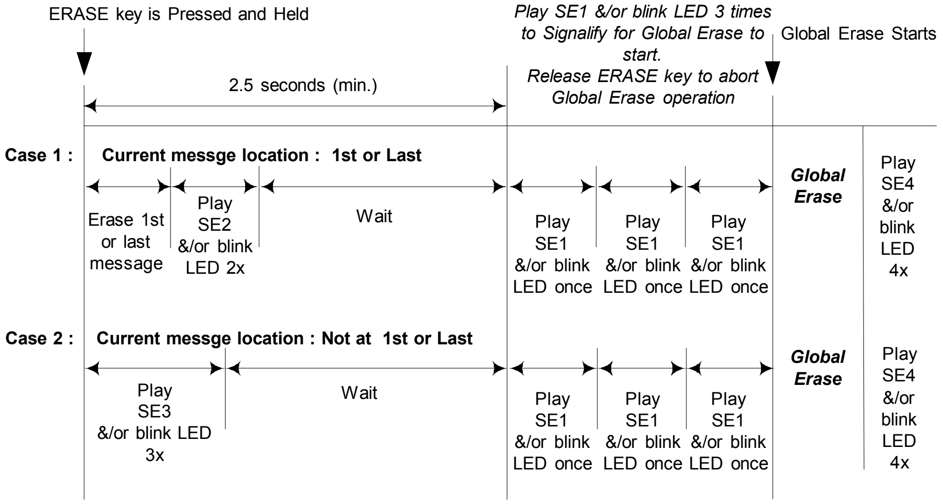

ERASE key is Pressed and Held
Play SE1 &/or blink LED 3 times to Signalify for Global Erase to start.
Release ERASE key to abort Global Erase operation
Global Erase Starts
2.5 seconds (min.)
Case 1 :
Current messge location : 1st or Last
Erase 1st or last message
Play SE2 &/or blink LED 2x
Wait
Play SE1 &/or blink LED once
Play SE1 &/or blink LED once
Play SE1 &/or blink LED once
Global Erase
Play SE4 &/or blink LED 4x
Case 2 :
Current messge location : Not at 1st or Last
Play SE3 &/or blink LED 3x
Wait
Play SE1 &/or blink LED once
Play SE1 &/or blink LED once
Play SE1 &/or blink LED once
Global Erase
Play SE4 &/or blink LED 4x

Figure 8.1: Global Erase Operation

8.2.5 Reset Operation

A 0.1 µF capacitor is recommended to connect the $\overline{\textbf{RESET}}$ to ground if a push button switch is used on this control. After $\overline{\textbf{RESET}}$ is triggered, the device will be in power down state and place both the record and the playback pointers at the last message. When a microcontroller is used for a power-on-Reset, $\overline{\textbf{RESET}}$ must stay active for at least 1 µsec after all supply rails reach their proper specifications.

8.2.6 VOL Operation

Pulsing $\overline{\text{VOL}}$ Low changes the volume output. Each pulse on $\overline{\text{VOL}}$ will decrease the volume until the minimum setting is reached. Subsequent pulses will increase the volume until the maximum level is reached and the cycle will start again. There are 8 steps of volume control. Each step changes the volume by 4 dB. The $\overline{\text{VOL}}$ is debounced internally. A $\overline{\text{RESET}}$ operation will re-initialize the volume level to the factory default state, which is the maximum level. One can change this default setting using related SPI command.

8.2.7 FT (Feed-Through) Operation

The $\overline{\text{FT}}$ controls the feed-through path from the input to the output of the chip. By factory default, when $\overline{\text{FT}}$ is held Low, FT mode is enabled. Active FT mode will pass AnaIn signal to both SPK and AUD outputs when the device is idle. During recording, device will record the AnaIn signal into the memory.

However, the FT path is subject to the contents of NVCFG register during power-on-reset. Once power-up, one can configure the feed-through path by changing the setting of the APC register using the related SPI commands.

8.3 vALERT FEATURE (OPTIONAL)

If this optional feature is enabled, after a recording operation, the LED output will blink once every few seconds to indicate the presence of a new message, while the device is in power-down state. After any subsequent operations, which power-up the device, the vAlert will stop flashing.

8.4 ANALOG INPUTS

8.4.1 Microphone Input

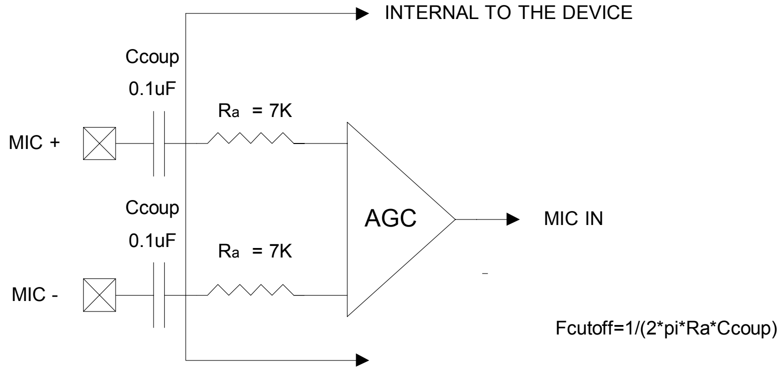


Figure 8.2: MIC input impedance (When this path is active)

8.4.2 AnaIn Input

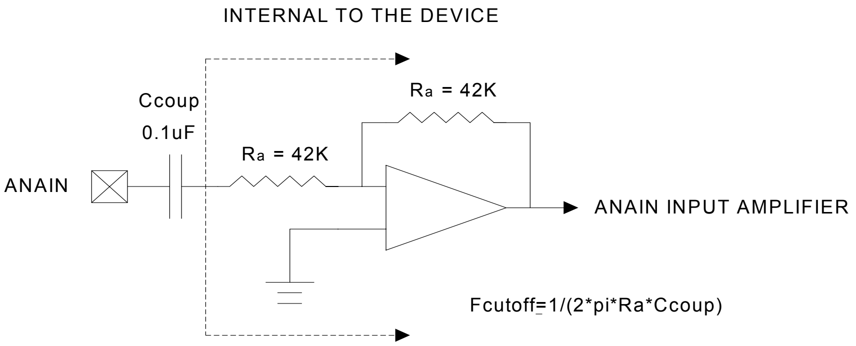


Figure 8.3: AnaIn input impedance (When the device is powered-up)

8.5 SYSTEM MANAGEMENT

While in Standalone mode, it is recommended the designer to utilize the feedback from the RDY/$\overline{\text{INT}}$ pin, visual and optional SE indications for effective system management with respect to its operations.

9 CIRCULAR MEMORY ARCHITECTURE (CMA)

The ISD1700 has a built-in circular memory management protocol to handle message management internally in Standalone mode. Before the device attempts to access memory via push-button controls or the SPI equivalent commands, it checks the memory structure for conformity to this circular memory protocol. If it fails, the LED will flash seven times and the device accepts no commands except reset and global erase in standalone mode. The only way to recover from this condition is to perform a global erase function successfully.

The area of memory under circular memory management control is from address 0x010 to the end of memory, i.e. only for the voice message storage. This is because the first sixteen rows, up to address 0x00F are reserved for sound effects (SE). When the address pointer reaches the end of the memory, it will automatically roll over to address 0x010. To comply with the circular memory architecture, all messages must form a contiguous block with no empty space between them and there must be at least one blank row left between the last message and first message. This allows ISD1700 state machine to find the first and last message in memory after POR or Chk_Mem command in SPI mode. This CMA is automatically implemented by the ISD1700 in standalone mode and the similar push-button SPI commands.

In SPI mode, however, the user has the option of direct addressing the array with the SET_PLAY, SET_REC and SET_ERASE commands, which are capable of going around this structure. This is an advantage if the user wishes to implement a fragmented memory management scheme onto the ISD1700. These SET commands also permit the recording, playback and erasing the sound effects in SPI mode. The SET_PLAY command can never corrupt the CMA, but the SET_REC and SET_ERASE commands have the ability to fragment the message memory area and invalidate the circular memory structure. Thus, if standalone operation or internal memory management is required, care must be taken in using these commands while in SPI mode.

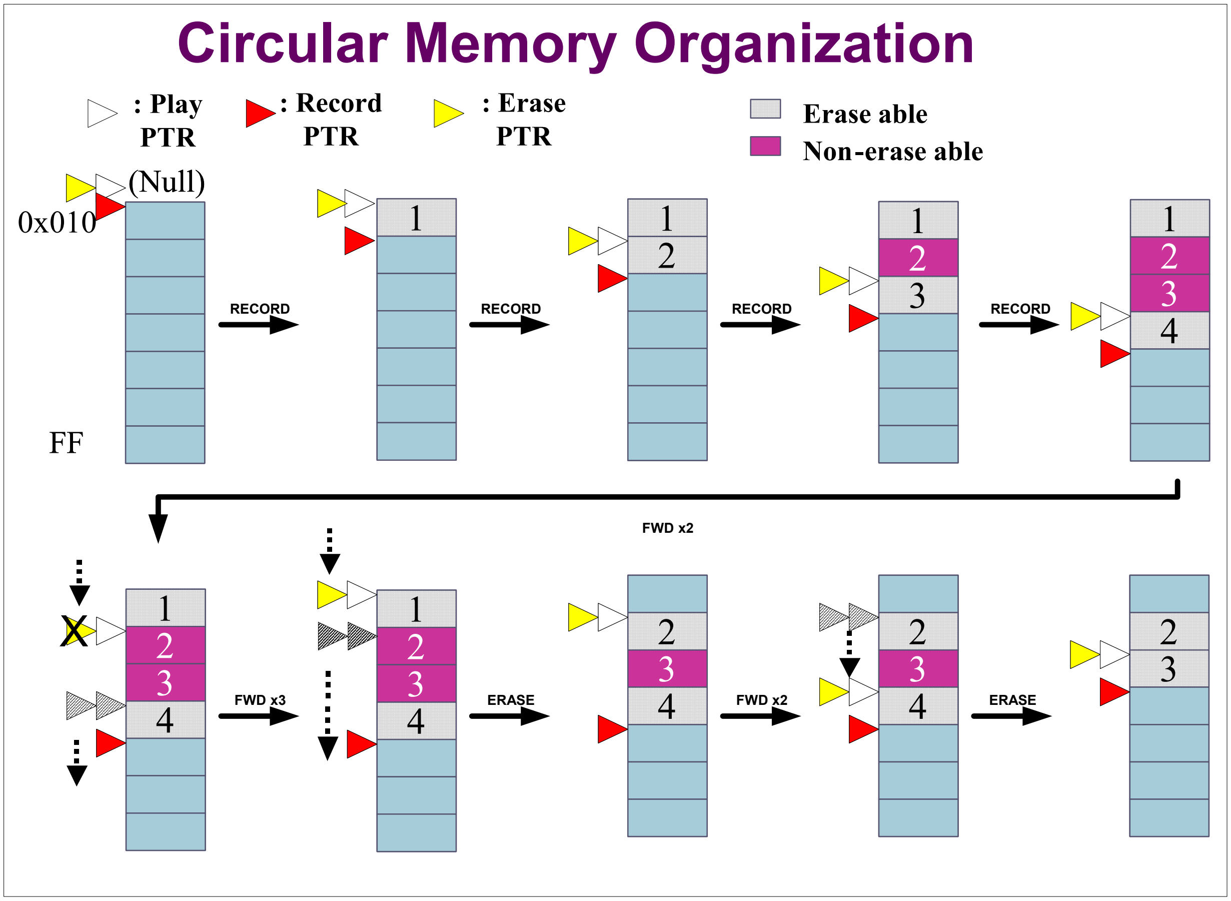


Figure 9.1 Circular Memory Management

An example of the Circular memory management is shown in Figure 9.1. Here the memory array starts with an empty memory, the ISD1700 detects this and sets the record pointer to point at row 0x010, the first row of normal memory. A subsequent REC command will record message 1. Now the playback pointer will point to the beginning of message 1 and the record pointer to the next row after message 1. Three more recordings will write message 2, 3 and 4. This results the record and playback pointers are at next row after message 4 and beginning of message 4, respectively. If two FWD commands are now sent, the playback pointer will jump from last message to message 1 then message 2. Note that the erase pointer is now invalid since erase is restricted to only the first or last message. If three FWD commands were executed, the playback pointer would end up back at message 1 after wrapping around the last message. Because the pointer is at the first message an erase command is valid. An ERASE will remove message 1 from the memory. Note that the record pointer has been unaffected by all these operations. A further two FWD and a subsequent ERASE commands will remove message 4.

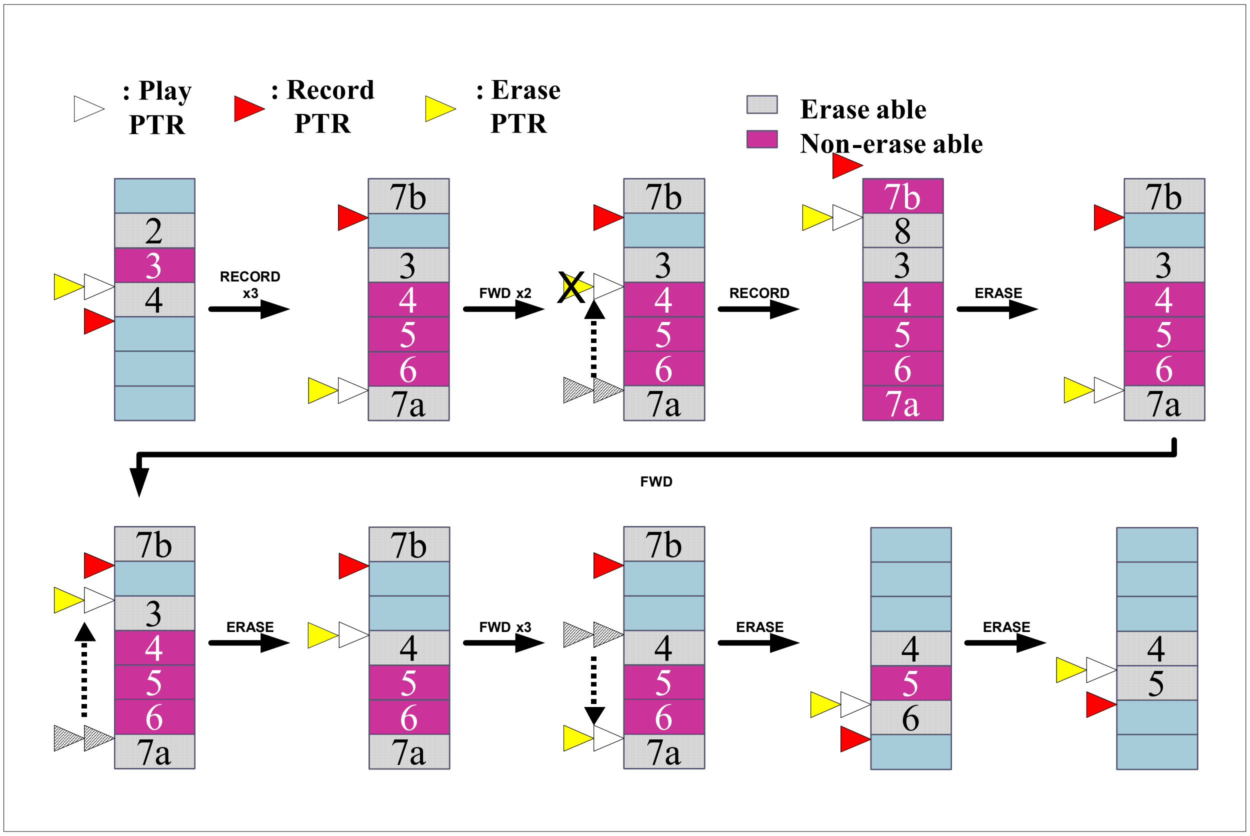


Figure 9.2 Further Circular Message Management

A Further example of circular memory management is shown in Figure 9.2. Here note how the three REC commands cause message 7 to be split across the end of memory boundary. Two FWD commands will wrap the playback pointer to message four – the second message in the circular queue. Now if we record until the memory is full, the record pointer becomes invalid and no further record commands will be accepted by the device. Either the first or last message must be erased first. The example above demonstrates erasing the last and then the first message as well.

9.1 RESTORING CIRCULAR MEMORY ARCHITECTURE

In case the circular memory architecture is damaged, the LED will blink seven times of duration T_{LErr} when either $\overline{\textbf{REC}}$, $\overline{\textbf{PLAY}}$, $\overline{\textbf{ERASE}}$ or $\overline{\textbf{FWD}}$ button or alike SPI commands are activated. During such occurrence, the only way to recover back to an operating status is to perform a successful global erase operation. In order to perform this effectively, one has to press-and-hold the $\overline{\textbf{ERASE}}$ for approximately twelve seconds (time for LED to blink seven times plus period for global erase) at 8 kHz sampling frequency. As a result, the device will resume back to the normal condition. Details are shown in the related timing diagram.

10 SERIAL PERIPHERAL INTERFACE (SPI) MODE

10.1 MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO & $\overline{SS}$) SPI interface can be used for serial communication to the ISD1700 device. The ISD1700 Series is configured to operate as a peripheral slave device. All operations can be controlled through this SPI interface.

To allow compatibility with Standalone mode, some SPI commands: PLAY, REC, ERASE, FWD, RESET and G_ERASE behave similarly as the corresponding features in Standalone mode. In addition, SET_PLAY, SET_REC and SET_ERASE commands allow the user to specify the start and the end addresses of the operation. Besides, there are commands accessing the APC register, which controls the configuration of the analog paths used by the device, and etc.

10.2 SPI INTERFACE OVERVIEW

The ISD1700 series operates via the SPI serial interface with the following protocol.

Data transfer protocol requires that the microcontroller's SPI shift registers are clocked out on the falling edge of the SCLK. The SPI protocol of the ISD1700 device is as follows:

1. A SPI transaction is initiated on the falling edge of the $\overline{SS}$ pin.
2. $\overline{SS}$ must be held Low during the entire data transfer process.
3. Data is clocked into the device through the MOSI pin on the rising edge of the SCLK signal and clocked out of the MISO pin on the falling edge of the SCLK signal, with LSB first.
4. The opcodes contain command, data and address bytes, depending upon the command type.
5. While control and address data are shifted into the MOSI pin, the status register and current row address are simultaneously shifted out of the MISO pin.
6. The SPI transaction is completed by raising the $\overline{SS}$ to High.
7. After completing an operational SPI command, an active Low interrupt is generated. It will stay Low until it is reset by the CLR_INT command.

10.2.1 SPI Transaction Format

Figure 10.1 describes the format of the SPI transaction. Data are shifted into the device on the MOSI data line. Concurrently, the device status and current row address and other data are returned to the host via the MISO data line. In order to perform functions normally, correct numbers of data bytes are required to shift into the MOSI. Meanwhile, the related numbers of bytes of information are shifted out from MISO.

LSB MSB

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte
MOSI	CMD_Byte	Data Byte 1	Data Byte 2 or Start Address (Low Byte)	Data Byte 3 or Start Address (High Byte)	End Address (Low Byte)	End Address (Mid Byte)	End Address (High Byte)

LSB MSB

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte
MISO	Status Register 0 (SR0) (Low Byte & High Byte)		Data Byte 1 or SR0 (Low Byte)	Data Byte 2 or SR0 (High Byte)	SR0 (Low Byte)	SR0 (High Byte)	SR0 (Low Byte)

Figure 10.1 SPI Transaction Format

10.2.2 MOSI Data Format

MOSI is the **M**aster **O**ut **S**lave **I**n data line of the SPI interface. Data is clocked into the device on the rising edge of the SCLK signal, with the least significant bit (LSB) first. Depending upon the command type, the format may be two bytes or as long as seven bytes. The generalized sequence of MOSI data is shown in the table below. The first byte sent to the device is always the command opcode byte, which determines the operation to be performed. Bit 4 (C4) of the command byte determines whether the LED feature is activated for related operations. When C4=1, the LED is On. Subsequent bytes are data associated with the type of command, which may include start and end addresses for operation or other data bits.

Table 10.1 MOSI Data Sequence

MSB	**1st Byte: Command Byte**						***LSB***
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C7	C6	C5	C4	C3	C2	C1	C0
MSB	**2nd Byte: Data Byte1**						***LSB***
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
X/D7	X/D6	X/D5	X/D4	X/D3	X/D2	X/D1	X/D0
MSB	**3rd Byte: Data Byte2 / Start Address Byte1**						***LSB***
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
X/S7	X/S6	X/S5	X/S4	D11/S3	D10/S2	D9/S1	D8/S0
MSB	**4th Byte: Data Byte3 / Start Address Byte2**						***LSB***
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
X	X	X	X	X	S10	S9	S8
MSB	**5th Byte: End Address Byte1**						***LSB***
Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
E7	E6	E5	E4	E3	E2	E1	E0
MSB	**6th Byte: End Address Byte2**						***LSB***
Bit 47	Bit 46	Bit 45	Bit 44	Bit 43	Bit 42	Bit 41	Bit 40
X	X	X	X	X	E10	E9	E8
MSB	**7th Byte: End Address Byte3**						***LSB***
Bit 55	Bit 54	Bit 53	Bit 52	Bit 51	Bit 50	Bit 49	Bit 48
X	X	X	X	X	X	X	X

Note: X = Don't care (Recommend 0)

Majority of commands are two-byte commands. The DEV_ID, RD_STATUS and WR_APC command are three-byte, in which the 2nd and 3rd bytes are data for WR_APC. The, RD_APC and Read pointer commands are four-byte. However, SET commands are seven-byte with Start address <S10:S0> and End address <E10:E0> and the rest address bits are reserved for future use (recommend 0). Address count starts at address 0x000, which is the start location of the first Sound Effect. Address locations 0x000-0x00F inclusively are reserved equally for 4 sound effects. Address 0x010 is the first address of non-reserved storage. For minimum storage resolution, please refer to Section 6.2.

10.2.3 MISO Data Format

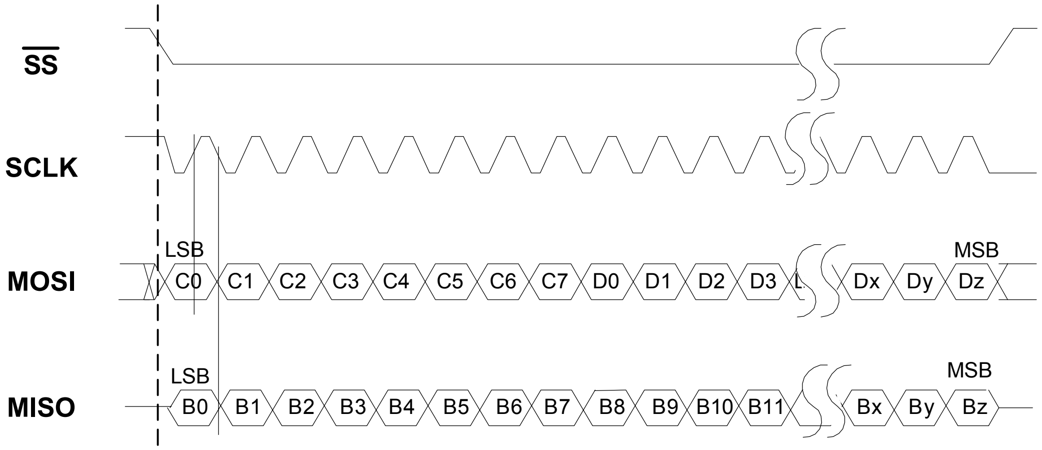
Data is clocked out of the **M**aster **I**n **S**lave **O**ut pin of ISD1700 device on the falling edge of the SCLK signal, with LSB first. MISO returns the status generated by the last command and current row address <A10:A0> in the first two bytes for all operations. The commands RD_STATUS, DEVID, RD_PLAY_PNTR, RD_REC_PNTR and RD_APC provide additional information in the subsequent bytes (see below sections for more details). The sequence of MISO is shown in the table below.

Table 10.2 MISO Data Sequence

LSB			**1st Byte : Status Register 0 (Low Byte)**				***MSB***
Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
CMD_ Err	Memory Full	Power Up	EOM	Interrupt	A0	A1	A2
LSB			**2nd Byte : Status Register 0 (High Byte)**				***MSB***
Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
A3	A4	A5	A6	A7	A8	A9	A10
LSB			**3rd Byte : Data Byte 1 or SR0 (Low Byte)**				***MSB***
Bit 16	Bit 17	Bit 18	Bit 19	Bit 20	Bit 21	Bit 22	Bit 23
D0 / CMD_ Err	D1/ Memory Full	D2 / Power Up	D3 / EOM	D4 / Interrupt	D5 / A0	D6 / A1	D7 / A2
LSB			**4th Byte : Data Byte 2 or SR0 (High Byte)**				***MSB***
Bit 24	Bit 25	Bit 26	Bit 27	Bit 28	Bit 29	Bit 30	Bit 31
D8 / A3	D9 / A4	D10 / A5	D11 / A6	D12 / A7	D13 / A8	D14 / A9	D15 / A10
LSB			**5th Byte : SR0 (Low Byte)**				***MSB***
Bit 32	Bit 33	Bit 34	Bit 35	Bit 36	Bit 37	Bit 39	Bit 39
CMD_ Err	Memory Full	Power Up	EOM	Interrupt	A0	A1	A2
LSB			**6th Byte : SR0 (High Byte)**				***MSB***
Bit 40	Bit 41	Bit 42	Bit 43	Bit 44	Bit 45	Bit 46	Bit 47
A3	A4	A5	A6	A7	A8	A9	A10
LSB			**7th Byte : SR0 (Low Byte)**				***MSB***
Bit 48	Bit 49	Bit 50	Bit 51	Bit 52	Bit 53	Bit 54	Bit 55
CMD_ Err	Memory Full	Power Up	EOM	Interrupt	A0	A1	A2

The status bits of the 1st byte provide important information on the result of the previous command sent. In particular, bit 0 (command error bit) indicates whether the chip is able to process the previous command or not. The address bits <A10:A0> represent the address location. The contents of the Data Bytes 1 & 2 are depended upon the previous command. The 5th, 6th and 7th bytes are the repeat of SR0 status.

SPI Format



where Cn & Dn represent input data bit of MOSI, while Bn are output data bit.

The initial condition of the SPI inputs to the ISD1700 should be:

- $\overline{\text{SS}}$ = High
- SCLK = High
- MOSI = Low

10.3 SPI Command Overview

The SPI commands offer greater control over the device than that in standalone mode. There are several types of commands:-

- Priority commands:
  - Accepted at any time and do not require state machine intervention.
  - PU, STOP, PD, RD_STATUS, CLR_INT, DEVID, RESET
- Circular memory commands:
  - Execute operations similar to in Standalone mode.
  - PLAY, REC, FWD, ERASE, G_ERASE, RD_REC_PTR, RD_PLAY_PTR
- Analog configuration commands:
  - Enable/disable various configuration paths, load/write APC and NVCFG registers, etc.
  - RD_APC, WR_APC, WR_NVCFG, LD_NVCFG, CHK_MEM,
- Direct memory access commands:
  - Execute operations with start and end addresses.
  - SET_ERASE, SET_REC, SET_PLAY

A SPI command always consists of a command byte. The command byte has one special purpose bit, bit 4 (LED). This bit controls the operation of the LED output. If the user wishes to enable the operation of the LED, all opcodes should have this bit set to 1.

In SPI mode, the memory location is fully accessible via row address. The microcontroller (μC) can access any rows including the reserved Sound Effect rows (0x000-0x00F). The SET_PLAY, SET_REC, and SET_ERASE commands require a specified start address and end address. If start address and end address are the same, ISD1700 will perform the operation on that row only. The SET_ERASE operation erases all rows specified by start address and end address inclusively. The SET_REC operation begins recording from start address and ends recording at end address, also writes an EOM marker at the end address. The SET_PLAY operation plays back message from start address and stops at end address.

Additionally, SET_PLAY, SET_REC, and SET_ERASE commands have a one deep FIFO buffer to offer seamless transitions from one block of memory to the next. This deep FIFO buffer is only valid for same type of SET commands, i.e. SET_PLAY followed by SET_ERASE will not utilize the buffer and a command error will be generated. The RDY bit in Status Register 1 will indicate when the chip is ready to accept the second command. Also, interrupt will be issued when the operation is completed. For example, if two consecutive SET-PLAY commands with two different pairs of addresses are sent correctly, then the buffer is full. After completing playback of the first message and the 1st SET_PLAY operation encounters an EOM, it will ignore the normal action for EOM, i.e. stop playback. Instead the device continues to execute the 2nd SET_PLAY command. As a result, the chip will playback the second message. This action will minimize any potential dead time between two recorded messages and allow the device to concatenate two individual messages smoothly.

If circular memory architecture is satisfied, one can use PLAY, REC, FWD, RESET, ERASE and G_ERASE commands, which will function similarly as the $\overline{\textbf{REC}}$, $\overline{\textbf{PLAY}}$, $\overline{\textbf{FWD}}$, $\overline{\textbf{RESET}}$, $\overline{\textbf{ERASE}}$ and global-erase in standalone mode, respectively. These commands will ensure that memory organization remain compatible with standalone operations. However, sound effects will not be activated like in standalone mode. If one wishes to switch between SPI and standalone modes, care must be taken in using SET_REC and SET_ERASE to follow the circular memory architecture.

10.4 Switching from SPI mode to Standalone Mode

While doing so, the following precautions have to be taken into account due to the circular memory architecture. First, the arrangement of messages created in SPI mode must match the circular memory structure. Second, only one empty slot is allowed inside the memory array. Third, the device must be “Reset” either before or after exiting the SPI mode, prior to any standalone functions being performed. Failure to do so will cause malfunctioning in standalone mode. As a result, LED will flash seven times. When happened, restoring circular memory architecture must be required.

10.5 ISD1700 Device Registers

There are several registers returning the internal state of the ISD1700 device. The following describes each and its access mode.

10.5.1 Status Register 0 (SR0)

SR0 is a two bytes data returning from MISO, which includes 5 status bits (D4:D0) and 11 address bits (A10:A0).

SR0		Size:	16 bits		Type:	Read			
Byte #1	Bit # :	D7	D6	D5	D4	D3	D2	D1	D0
	Name :	A2	A1	A0	INT	EOM	PU	FULL	CMD_ERR
Byte #2	Bit # :	D15	D14	D13	D12	D11	D10	D9	D8
	Name :	A10	A9	A8	A7	A6	A5	A4	A3
	Description:	Device status register							
	Access	Every SPI command returns SR0 as first two bytes in MISO							

Table 10.3 Bit description of Status Register 0

SR0			
	Bit	Name	Description
Byte #1	7	A2	Current row address bit 2
	6	A1	Current row address bit 1
	5	A0	Current row address bit 0
	4	INT	This bit is set to 1 when current operation is done. It can be cleared by CLR_INT command.
	3	EOM	This bit is set to 1 when an EOM is detected. It can be cleared by CLR_INT command.
	2	PU	This bit is set to 1 when the device is powered up and operating in SPI mode.
	1	FULL	This bit, when set to 1, indicates memory array is full. That means the device cannot record any new messages unless old messages are deleted. This bit is only valid when user follows push button format to program and erase the array.
	0	CMD_ERR	This bit indicates the previous SPI command is invalid when is set to 1, if: µC sends less than 5 bytes of row address, SPI command is decoded but ignored.
Byte #2	15	A10	Current row address bit 10
	14	A9	Current row address bit 9
	13	A8	Current row address bit 8
	12	A7	Current row address bit 7
	11	A6	Current row address bit 6
	10	A5	Current row address bit 5
	9	A4	Current row address bit 4
	8	A3	Current row address bit 3

where <A10:A0> is the active row of memory

10.5.2 Status Register 1 (SR1)

SR1	Size:	8 bits	Type:	Read			
Bit Sequence:	D7	D6	D5	D4	D3	D2	D1	D0
	SE4	SE3	SE2	SE1	REC	PLAY	ERASE	RDY
Description:	Device secondary status register							
Access	RD_STATUS command. <D7:D0> is the third byte of MISO							

Table 10.4 Bit description of Status Register 1

SR1		
Bit	Name	Description
7	SE1	This bit is set to 1 when sound effect 1 is recorded and 0 when erased
6	SE2	This bit is set to 1 when sound effect 2 is recorded and 0 when erased
5	SE3	This bit is set to 1 when sound effect 3 is recorded and 0 when erased
4	SE4	This bit is set to 1 when sound effect 4 is recorded and 0 when erased
3	REC	This bit (=1) indicates current operation is recording
2	PLAY	This bit (=1) indicates current operation is playback
1	ERASE	This bit (=1) indicates current operation is erase
0	RDY	In standalone mode, RDY=1 indicates the device is ready to accept command. In SPI mode, SPI is ready to accept new command, if this bit equals to 1. For REC, PLAY or ERASE, if RDY=0 means the device is busy and will not accept a new command, except RESET, CLR_INT, RD_STATUS, PD. However, REC and PLAY will also accept STOP command. If other commands are sent, they will be ignored and CMD_ERR will be set to 1. For any SET commands, RDY=1 means the buffer is empty, SPI can accept similar SET command. If host sends other commands, SPI will ignore it and set CMD_ERR to 1 unless new commands are RESET, CLR_INT, RD_STATUS, and PD. Also, SET_REC and SET_PLAY will accept STOP command.

10.5.3 APC Register

APC	Size:	12 bits	Type:	R/W
Bit Sequence:	<D11:D0> (See **Table 7.1**)			
Description:	Analog Path Configuration register.			
Access	Read: RD_APC; Write: LD_APC			

10.5.4 Playback Pointer (PLAY_PTR)

PLAY_PTR	Size:	11 bits	Type:	Read
Bit Sequence:	PLAY_PTR <A10:A0>			
Description:	Pointer at beginning of current message			
Access	Read: RD_PLAY_PTR; Changed by FWD, RESET, REC			

10.5.5 Record Pointer (REC_PTR)

REC_PTR	Size:	11 bits	Type:	Read
Bit Sequence:	REC_PTR <A10:A0>			
Description:	Pointer at first available row in the memory.			
Access	Read: RD_REC_PTR; Changed by REC			

10.5.6 DEVICEID Register

DEVICEID	Size	8 bits	Type	Read				
Bit Sequence:	D7	D6	D5	D4	D3	D2	D1	D0
	CHIPID					Reserved		
Description:	Device identification register							
Access	DEVID command as third byte of MISO							

Table 10.5 Bit description of DEVICEID Register

DEVICEID			
Bits	Name	Description	
<7:3>	CHIPID	DDDDD 76543	Device
		11100	ISD17240
		11101	ISD17210
		11110	ISD17180
		11000	ISD17150
		11001	ISD17120
		11010	ISD1790
		10100	ISD1760
		10101	ISD1750
		10110	ISD1740
		10000	ISD1730
<2:0>	Reserved	Reserved	

11 SPI COMMAND REFERENCE

This section describes the SPI command set. A summary of commands is given in Table 11.1 and commands are detailed in subsequent sub-sections.

Table 11.1 SPI Command Reference

Instructions [1]	**Command Byte** [2]	**Data Byte1**	**Data Byte2 or Start Address Byte1** [3]	**Data Byte3 or Start Address Byte2** [3]	**End Address Bytes 1/2/3** [3]	**Description**
PU	0x01	0x00				
STOP	0x02	0x00				Stop the current operation
RESET	0x03	0x00				Reset the device
CLR_INT	0x04	0x00				Clear interrupt and EOM bit
RD_STATUS	0x05	0x00	0x00			Returns status bits & current row counter in first 1st 2 bytes and operating status in 3rd byte
RD_PLAY_PTR	0x06	0x00	0x00	0x00		Returns status bits & current row counter in 1st 2 bytes and playback pointer in 3rd & 4th bytes
PD	0x07	0x00				Power down the device
RD_REC_PTR	0x08	0x00	0x00	0x00		Returns status bits & current row counter in 1st 2 bytes and Record pointer in 3rd & 4th bytes
DEVID	0x09	0x00	0x00			Read the device ID register.
PLAY	0x40	0x00				Play from current location without LED action until EOM or STOP command received
REC	0x41	0x00				Record from current location without LED action until end of memory or STOP command received
ERASE	0x42	0x00				Erase current message to EOM location
G_ERASE	0x43	0x00				Erase all messages (not include Sound Effects)

Instructions [1]	Command Byte [2]	Data Byte1	Data Byte2 or Start Address Byte1 [3]	Data Byte3 or Start Address Byte2 [3]	End Address Bytes 1/2/3 [3]	Description
RD_APC	0x44	0x00	0x00	0x00		Returns status bits & current row counter in first 1st 2 bytes and the contents of APC register in 3rd & 4th bytes.
WR_APC1	0x45	<D7:D0>	<xxxx D11:D8>			Write the data <D11:D0> into the APC register with volume setting from $\overline{\textbf{VOL}}$ pin
WR_APC2	0x65	<D7:D0>	<xxxx D11:D8>			Write the data <D11:D0> into the APC register with volume setting from bits <D2:D0>
WR_NVCFG	0x46	0x00				Write the contents of APC to NVCFG
LD_NVCFG	0x47	0x00				Load contents of NVCFG to APC Register
FWD	0x48	0x00				Forward playback pointer to start address of next message. Forward will be ignored during operating, except Play
CHK_MEM	0x49	0x00				Check circular memory
EXTCLK	0x4A	0x00				Enable/disable external clock mode
SET_PLAY	0x80	0x00	<S7:S0>	<xxxxx S10:S8>	<xxxx xxxx xxxxxE10:E0>	Play from start address <S10:S0> to end address <E10:E0> or stop at EOM, depending on the D11 of APC
SET_REC	0x81	0x00	<S7:S0>	<xxxxx S10:S8>	<xxxx xxxx xxxxxE10:E0>	Record from start address <S10-S0> to end address <E10:E0>
SET_ERASE	0x82	0x00	<S7:S0>	<xxxxx S10:S8>	<xxxx xxxx xxxxxE10:E0>	Erase from start address <S10:S0> to end address <E10:E0>

Note: [1] Set initial SPI condition as listed in Section 10.2 before any SPI command is sent.

[2] Bit C4 (LED) must be set to 1 if LED indication is required. During the active state of LED output, no new command will be accepted.

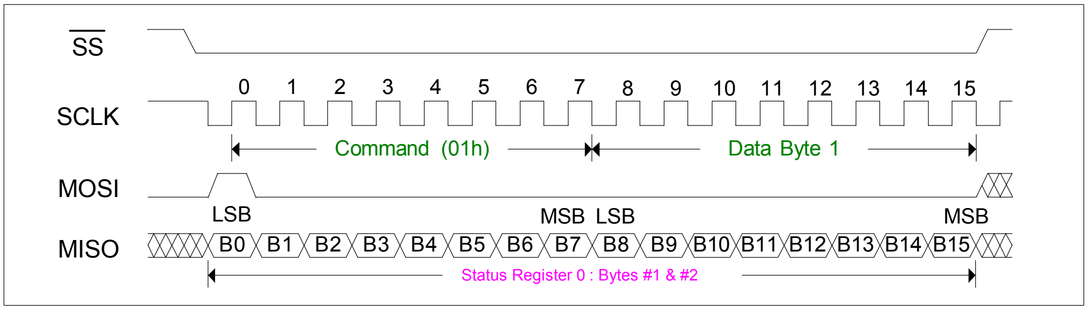
[3] For “xxx…”, recommend to use “000…”

Before starting to write the program code, one has to fully understand the definition of each command and how to implement each of them correctly. If not, you may end up to spend lots of time and efforts in debugging the program code. The following several sections illustrate exactly how the communication sequence of each SPI command should be. Bear in mind that the first bit of each input data byte shifting into the MOSI must be LSB, whereas the first bit of data byte coming out from the MISO is LSB. Also, care must be provided to fulfill the initial conditions on the $\overline{\textbf{SS}}$, SCLK and MOSI inputs (as shown in Section 10.2). If wrong format is sent, then the device may not response at all or may respond strangely. Also, not every command will generate an interrupt feedback signal to the host in responding to the operation requested. Thus, precautions must be well considered to ensure that the device is ready to accept a new instruction. Otherwise, the instruction sent will be ignored.

11.1 SPI PRIORITY COMMANDS

This class of SPI commands will always be accepted by the ISD1700. They control power up and down of the device, interrogating the status of the device and clearing interrupt requests.

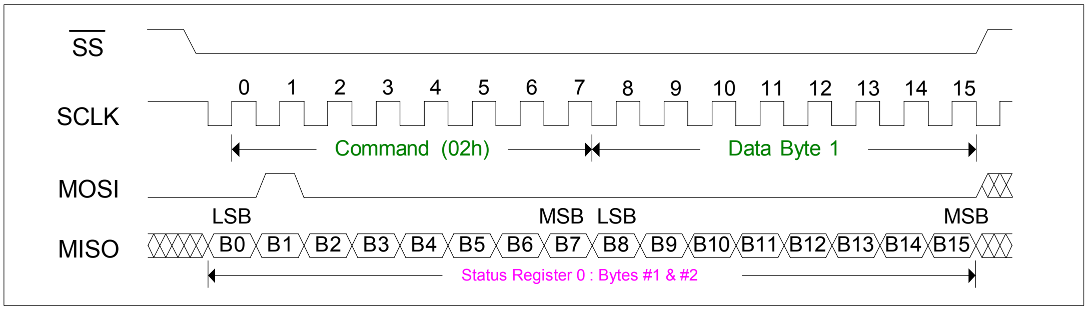
11.1.1 PU (0x01) Power Up



PU	Opcode:	0x01	0x00	Interrupt:	No	
Byte Sequence:	MOSI		0x01	0x00		
	MISO		SR0			
Description:	Power up					
State before Execution	Power Down					
State after Execution	Idle/FT					
Registers Affected	SR0: PU bit, SR1: RDY bit					

This command wakes up the ISD1700 device and enables it into the idle state. Upon executing this command, PU bit of SR0 and RDY bit of SR1 are set to 1. This command does not generate an interrupt. Once in SPI mode, the input from $\overline{\textbf{FT}}$ pin is ignored and its function is replaced by Bit 6 of the APC register. SPI mode is exited via a PD (power down) command.

11.1.2 STOP (0x02)

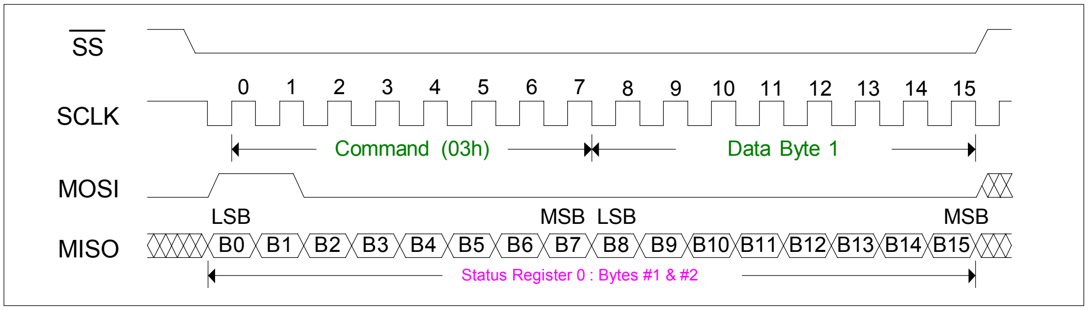


STOP	Opcode:	0x02	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x02	0x00		
	MISO		SR0			
Description:	Stop the current operation					
State before Execution	REC, PLAY, SET_PLAY, SET_REC					
State after Execution	Idle/FT					
Registers Affected	SR0: INT bit, SR1: RDY/PLAY/REC bits					

This command stops the current operation and returns the device back to the state prior to the operation. This command is only valid for the PLAY, REC, SET_PLAY and SET_REC operations. Upon completion, an interrupt is generated.

The CMD_ERR bit of SR0 is set when the STOP command is sent during ERASE, G_ERASE and SET_ERASE operations. As STOP is sent while the device is idle, no action is taken and no interrupt is generated.

11.1.3 RESET (0x03)

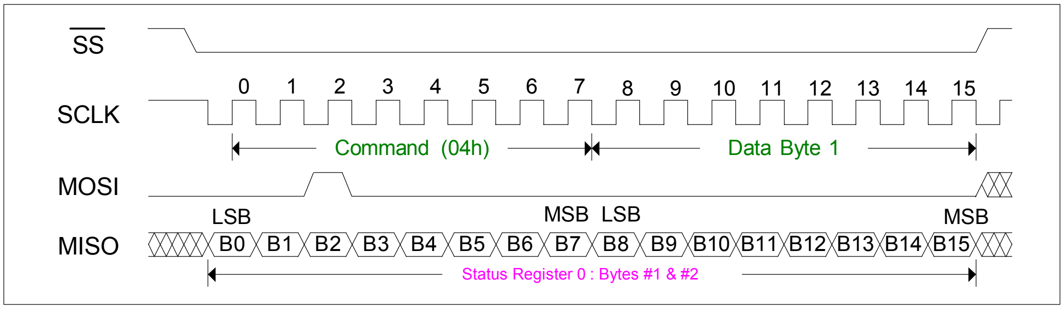


RESET	Opcode:	0x03	0x00	Interrupt:	No	
Byte Sequence:	MOSI		0x03	0x00		
	MISO		SR0			
Description:	Reset the Device					

State before Execution	Any, except PD
State after Execution	PD
Registers Affected	SR0, SR1, APC

This command stops the current operation, if any, puts the device back to power down state, and clears the status of interrupt & EOM bits. As a result, all interrupt & EOM bits are cleared and $\overline{\text{INT}}$ is released.

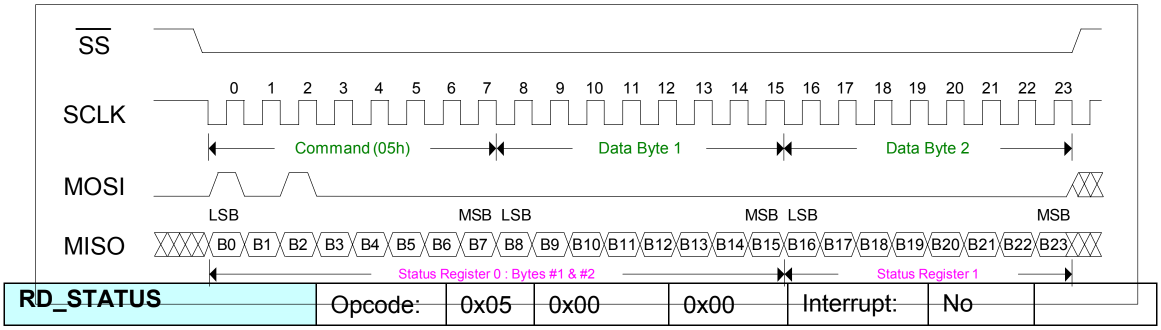
11.1.4 CLR_INT(0x04)



CLR_INT	Opcode:	0x04	0x00	Interrupt:	No
Byte Sequence:	MOSI	0x04	0x00		
	MISO	SR0			
Description:	Read Status and Clear INT and EOM				
State before Execution	Any				
State after Execution	Does not affect state, clears the INT bit and $\overline{\text{INT}}$ pin.				
Registers Affected	SR0: INT bit, EOM bit				

The Clear Interrupt command reads the status of the device and clears the status of interrupt & EOM bits. As a result, all interrupt & EOM bits are cleared and $\overline{\text{INT}}$ is released.

11.1.5 RD_STATUS (0x05)



RD_STATUS	Opcode:	0x05	0x00	0x00	Interrupt:	No	

Byte Sequence:	MOSI	0x05	0x00	0x00	
	MISO	SR0		SR1	
Description:	Read Status				
State before Execution	Any				
State after Execution	Does not affect state.				
Registers Affected	None				

The Read Status command reads the status of the device. This command has three bytes. See Table 10.3 and Table 10.4 for description of status register bits.

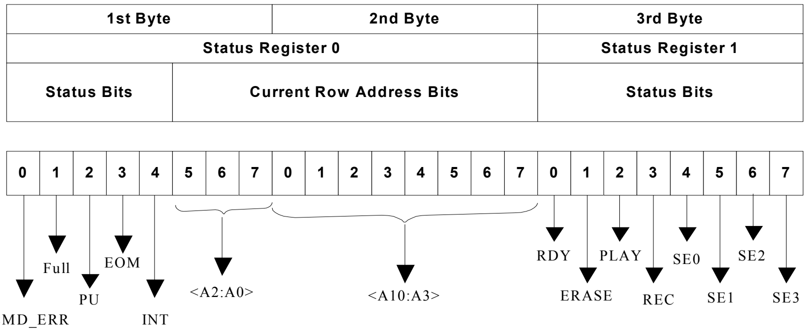
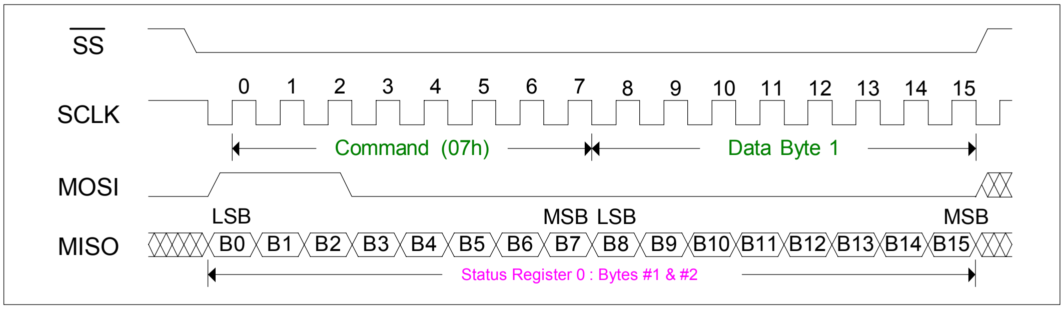


Figure 11.1 Status Read Command

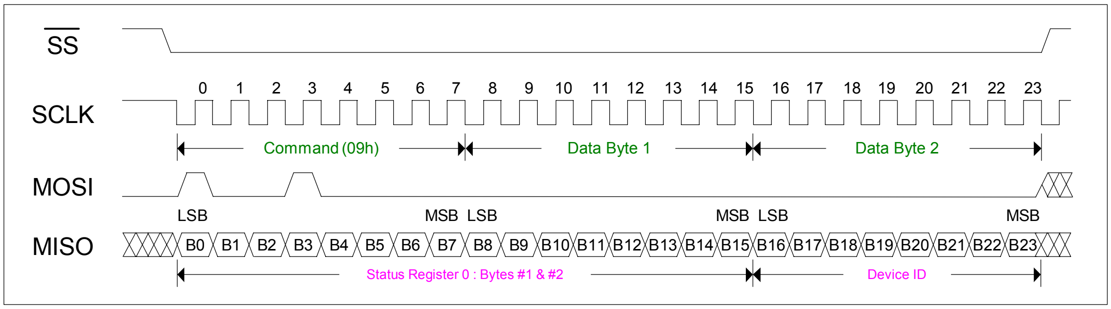
11.1.6 PD (0x07) Power Down



PD	Opcode:	0x07	0x00	Interrupt:	No
Byte Sequence:	MOSI		0x07	0x00	
	MISO		SR0		
Description:	Power down the device and enter into standby mode				
State before Execution	Any. If sent during a REC, PLAY or ERASE operation, device will finish operation before powering down.				
State after Execution	PD				
Registers Affected	SR0: PU bit				

This command places the ISD1700 into power-down mode and also enable standalone mode. If command is sent during an active play/record/erase operation, the device will first finish the current operation then power down. Upon completion, the device generates an interrupt. While exiting SPI mode, the $\overline{\text{INT}}$ /RDY pin status switches from $\overline{\text{INT}}$ to RDY state.

11.1.7 DEVID (0x09) Read Device ID



DEVID	Opcode:	0x09	0x00	Interrupt:	No	
Byte Sequence:	MOSI		0x09	0x00	0x00	
	MISO		SR0		DEVICEID	
Description:	Read the DEVICEID register to identify the device family					
State before Execution	Any					
State after Execution	Does not affect state.					
Registers Affected	None					

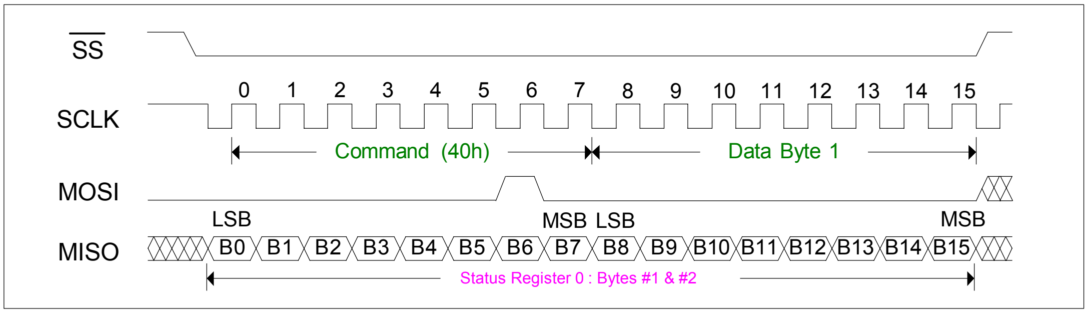
The Read Device ID command reads the ID register and returns the device name in the third byte of MISO to identify which device is present. See Table 10.5 for a description of DEVICEID register bits.

11.2 CIRCULAR MEMORY COMMANDS

A circular memory command performs a simple typical operation similar to the related function as in standalone mode except it does not automatically playback sound effects (SE) for audio feedback of the operation. So if sound effects are required to mimic the standalone operations, separate commands are needed to perform the features. These commands need to comply with the circular memory architecture. Before these commands are executed, the ISD1700 checks the memory structure first. If it does not match the circular memory architecture. then CMD_ERR bit in Status Register 0 (SR0) will be set to one and command will not execute.

In addition to the push-button similar commands, commands to read the record and playback pointers as well as to check whether current memory structure matches the circular memory architecture are available, thus allow the SPI host to track the locations of the recorded messages for its own message management.

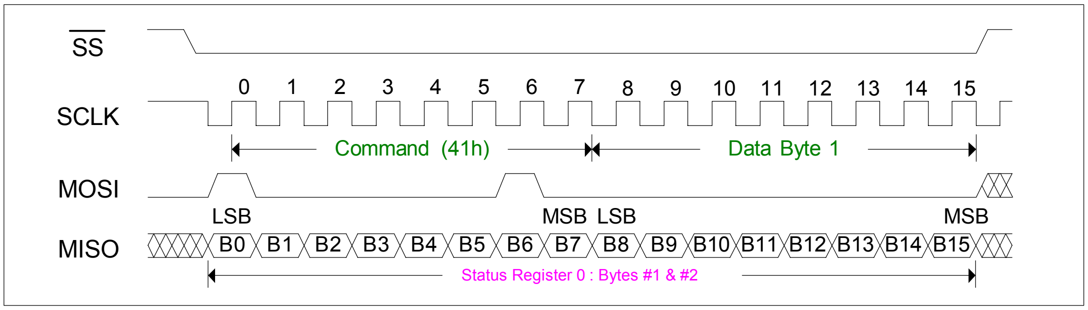
11.2.1 PLAY (0x40)



PLAY	Opcode:	0x40	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x40	0x00		
	MISO		SR0			
Description:	Device starts to playback from current PLAY_PTR					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	SR0, SR1: PLAY & RDY bits					

The PLAY command starts playback operation from current message and stops when it reaches EOM or receives STOP command. During playback, the device only responds to STOP, RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR of SR0 is set when other commands are sent. Both RDY and PLAY bits of SR1 are Low during PLAY.

11.2.2 REC (0x41)

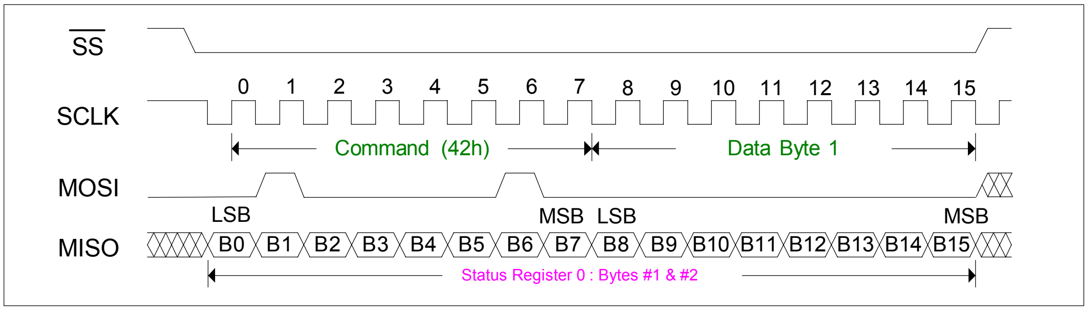


REC	Opcode:	0x41	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x41	0x00		
	MISO		SR0			
Description:	Device will record from current REC_PTR					
State before Execution	Idle					

State after Execution	Idle
Registers Affected	SR0, SR1: REC & RDY bits

The REC command starts record operation from current REC_PTR and stops when it receives STOP command or memory array is full. In record mode, the device only responds to STOP, RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR bit of SR0 is set while other commands are sent. Both RDY and REC bits of SR1 are Low during recording. Power supply must be remained during the entire operation.

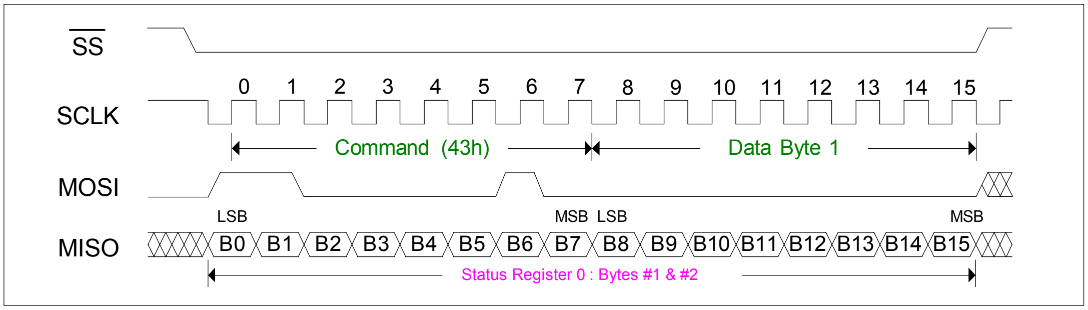
11.2.3 ERASE (0x42)



ERASE	Opcode:	0x42	0x00	Interrupt:	Yes	
Byte Sequence:	MOSI		0x42	0x00		
	MISO		SR0			
Description:	Device will delete the message from current message if at first or last message					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	SR0, SR1: ERASE & RDY bits					

The ERASE command erases the current message row by row when it is either the first or the last one. It stops when it reaches EOM. In erase mode, the device only responds to RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR bit of SR0 is set while other commands are sent or the current message is neither the first nor the last message. Both RDY and ERASE bits of SR1 are Low during erase. Power supply must be remained during the entire operation.

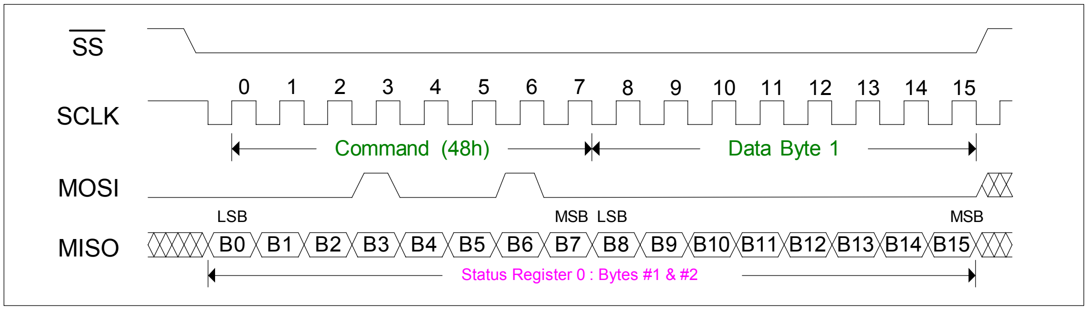
11.2.4 G_ERASE (0x43) Global Erase



G_ERASE	Opcode	0x43	0x00	Interrupt	Yes	
Byte Sequence:	MOSI		0x43	0x00		
	MISO		SR0			
Description:	Device will ERASE all messages.					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	SR0, SR1: ERASE & RDY					

The G_ERASE command deletes all messages within the entire memory array, except the SE portion (rows 0x000-0x00F), regardless the location of the PLAY_PTR. In the G_ERASE mode, the device only responds to RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR of SR0 is set when other commands are sent. Both the RDY and ERASE bits of SR1 are Low during erase process.

11.2.5 FWD (0x48)



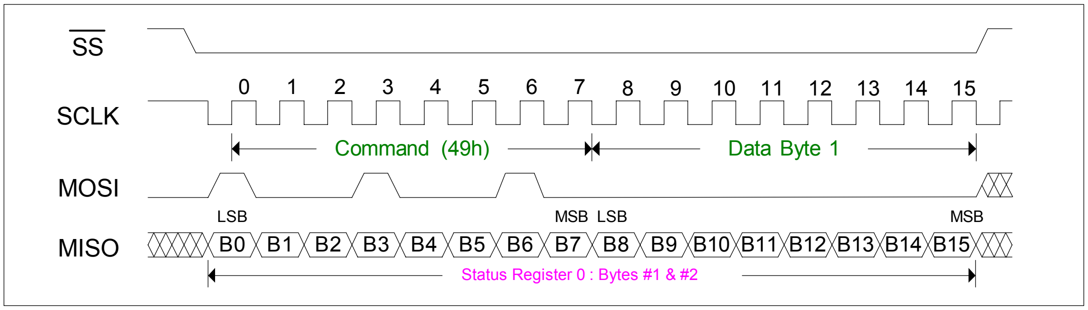
FWD	Opcode	0x48	0x00	Interrupt	Yes	
Byte Sequence:	MOSI		0x48	0x00		
	MISO		SR0			
Description:	Advances the PLAY_PTR to next message					
State before Execution	Idle					

State after Execution	Idle
Registers Affected	SR0, PLAY_PTR

This command enables the PLAY_PTR to jump from current address to the start address of next message. Unlike the $\overline{\textbf{FWD}}$ in standalone mode, FWD doesn't interrupt a current playback operation and can only be issued in the SPI idle state. To emulate a $\overline{\textbf{FWD}}$ during playback in standalone mode, the STOP command must first be issued, then followed by FWD and PLAY commands.

To determine the location of the PLAY_PTR, the RD_PLAY_PTR command can be used.

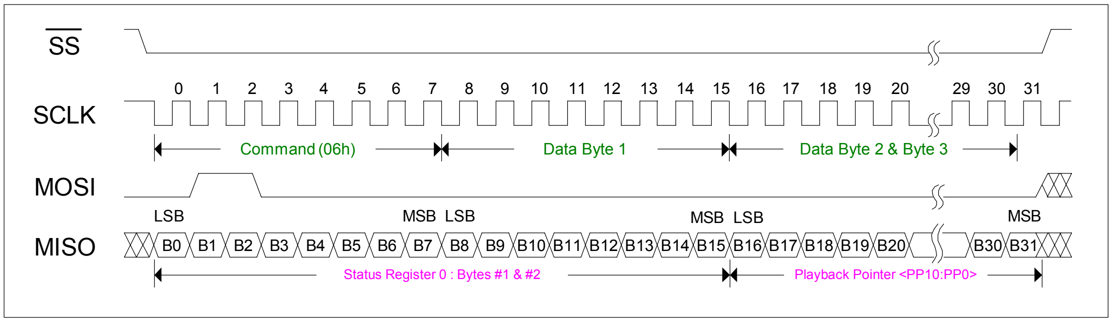
11.2.6 CHK_MEM (0x49) Check Circular Memory



CHK_MEM	Opcode	0x49	0x00	Interrupt	Yes	
Byte Sequence:	MOSI		0x49	0x00		
	MISO		SR0			
Description:	Check the validity of circular memory architecture					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	SR0, PLAY_PTR, REC_PTR					

The CHK_MEM command enables the device to check whether the arrangement of the messages conforms to circular memory architecture under standalone condition. The device must be powered up and in idle state for this command to operate. When existing memory structure fails circular memory check, the CMD_ERR of SR0 is set. Upon the successful completion, the record and playback pointers are initialized, i.e. the playback pointer points to the last message and the record pointer points to the first available memory row. The read pointer commands can now be used to determine the positions of both pointers. Also with the FWD command applied, the start address of the subsequent messages can be located.

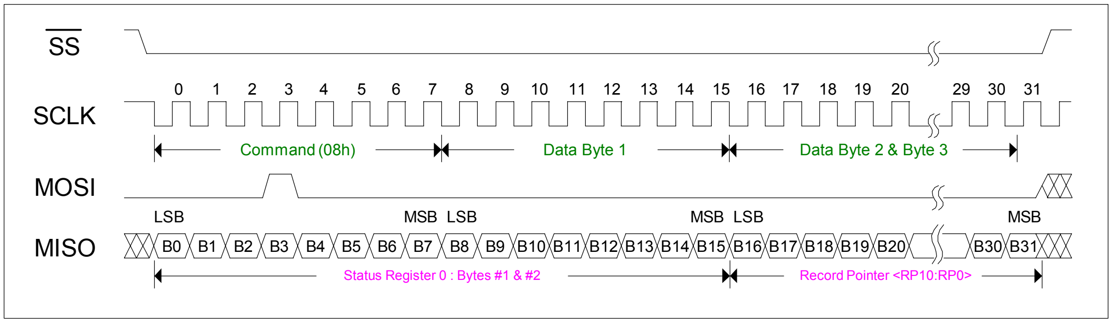
11.2.7 RD_PLAY_PTR (0x06)


SS
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 29 30 31
Command (06h)
Data Byte 1
Data Byte 2 & Byte 3
MOSI
LSB
MSB LSB
MSB LSB
MSB
MISO
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B30 B31
Status Register 0 : Bytes #1 & #2
Playback Pointer <PP10:PP0>

RD_PLAY_PTR	Opcode	0x06	0x00	Interrupt	No
Byte Sequence:	MOSI	0x06	0x00	0x00	0x00
	MISO	SR0		PP<7:0>	xxxxx PP<10:8>
Description:	Read the current position of the PLAY_PTR PP<10:0>.				
State before Execution	After CHK_MEM or idle				
State after Execution	Idle				
Registers Affected	None				

This command reads out the playback pointer address, where a push-button compatible playback or **PLAY** starts from. Prior sending this command, ensure circular memory architecture is satisfied by performing CHK_MEM. Otherwise, invalid data is obtained.

11.2.8 RD_REC_PTR (0x08)


SS
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 29 30 31
Command (08h)
Data Byte 1
Data Byte 2 & Byte 3
MOSI
LSB
MSB LSB
MSB LSB
MSB
MISO
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B30 B31
Status Register 0 : Bytes #1 & #2
Record Pointer <RP10:RP0>

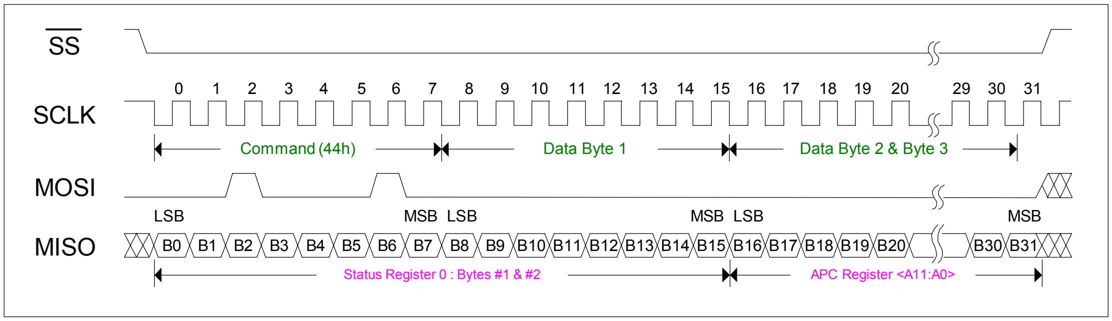
RD_REC_PTR	Opcode	0x08	0x00	Interrupt	No
Byte Sequence:	MOSI	0x08	0x00	0x00	0x00
	MISO	SR0		RP<7:0>	xxxxx RP<10:8>
Description:	Read the current position of the REC_PTR RP<10:0>.				
State before Execution	After CHK_MEM or idle				
State after Execution	Idle				
Registers Affected	None				

This command reads out the record pointer address, where a push-button compatible record or $\overline{\textbf{REC}}$ starts from. Prior sending this command, ensure circular memory architecture is satisfied by performing CHK_MEM. Otherwise, invalid data is obtained.

11.3 Analog Configuration Commands

These kind of commands allow the SPI host to configure the analog properties of the device.

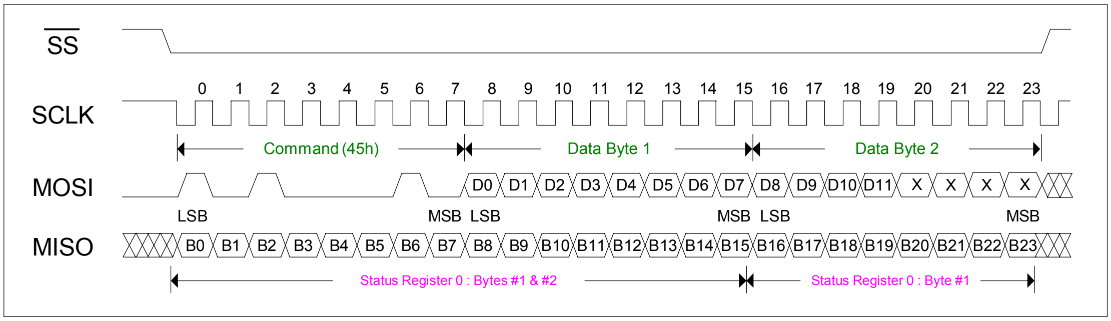
11.3.1 RD_APC (0x44) Read APC Register



RD_APC	Opcode	0x44	0x00	0x00	0x00	Interrupt	No
Byte Sequence:	MOSI	0x44	0x00	0x00	0x00		
	MISO	SR0		APC<7:0>	xxxxx APC<11:8>		
Description:	Read the current contents of the APC register.						
State before Execution	Idle						
State after Execution	Idle						
Registers Affected	None						

This command reads out the contents of APC register. After sending SR0, the device will send out the APC register data. This command has 4 bytes.

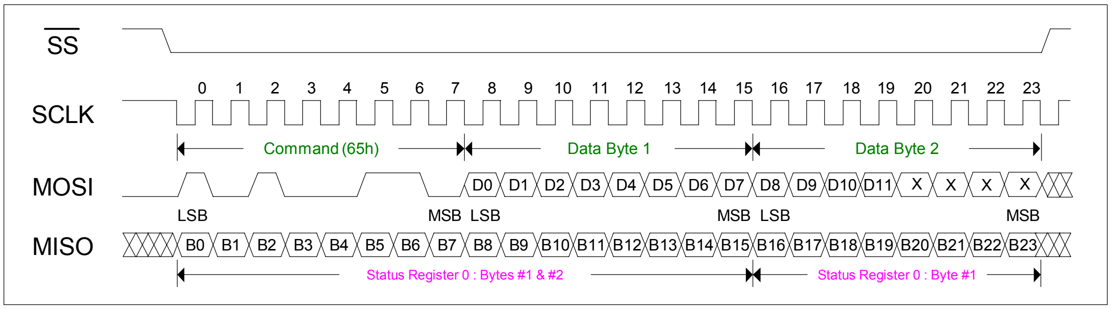
11.3.2 WR_APC1 (0x45) Load APC Register


SS
SCLK
MOSI
MISO
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
Command (45h)
Data Byte 1
Data Byte 2
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 X X X X
LSB
MSB LSB
MSB LSB
MSB
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23
Status Register 0 : Bytes #1 & #2
Status Register 0 : Byte #1

WR_APC1	Opcode	0x45	<D7:D0>	<D11:D8>	Interrupt	No
Byte Sequence:	MOSI	0x45	<D7:D0>	<xxxxxD11:D8>		
	MISO	SR0		SR0: 1st byte		
Description:	Load the data <D11:D0> to the APC register with volume setting from $\overline{\mathbf{VOL}}$ pin					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	APC					

The WR_APC1 command loads the desired data into the APC Register. There are three bytes involved: the first byte is command code, the second byte has data for APC<7:0> and the third byte contains APC<11:8>. The five most significant bits of the third byte are ignored. In this command, volume setting is from $\overline{\mathbf{VOL}}$ pin, rather than the VOL bits <D2:D0>. Care must be taken as changing the volume level if the device is executing an active command. Otherwise unintended transients may occur on the analog path.

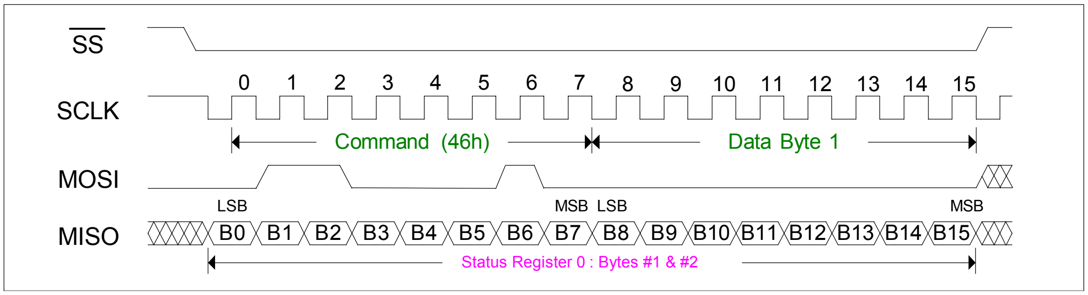
11.3.3 WR_APC2 (0x65) Load APC Register


$\overline{\text{SS}}$
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
Command (65h)
Data Byte 1
Data Byte 2
MOSI
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 X X X X
LSB
MSB LSB
MSB LSB
MSB
MISO
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23
Status Register 0 : Bytes #1 & #2
Status Register 0 : Byte #1

WR_APC2	Opcode	0x65	<D7:D0>	<D11:D8>	Interrupt	No
Byte Sequence:	MOSI	0x65	<D7:D0>	<xxxxxD11:D8>		
	MISO	SR0		SR0: 1st byte		
Description:	Load the data <D11:D0> to the APC register with volume setting from <D2:D0> bits					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	APC					

The WR_APC2 command loads the desired data into the APC Register. There are three bytes involved: the first byte is command code, the second byte has data for APC<7:0> and the third byte contains APC<11:8>. The five most significant bits of the third byte are ignored. In this command, volume setting is from the bits <D2:D0>, rather than $\overline{\mathbf{VOL}}$ pin. Care must be taken as changing the volume level if the device is executing an active command. Otherwise unintended transients may occur on the analog path.

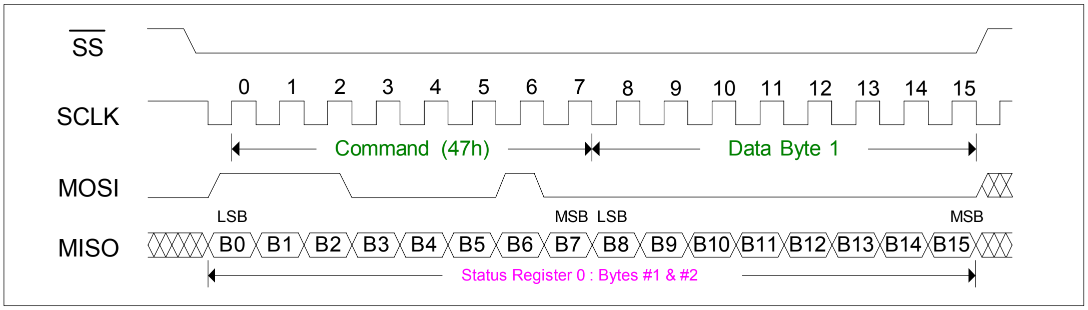
11.3.4 WR_NVCFG (0x46) Write APC data into Non-Volatile Memory



WR_NVCFG	Opcode	0x46	0x00	Interrupt	No	
Byte Sequence:	MOSI		0x46	0x00		
	MISO		SR0			
Description:	Write the current content of the APC register into the NVCFG register					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	None					

This command writes the data of the APC register into the NVCFG register. This value is loaded from NVCFG register to the APC register after a power-on condition or RESET. The CMD_ERR bit of SR0 is set if ISD1700 is not in idle state when this command is sent.

11.3.5 LD_NVCFG (0x47) Load APC register from Non-Volatile Memory



LD_NVCFG	Opcode	0x47	0x00	Interrupt	No	
Byte Sequence:	MOSI		0x47	0x00		
	MISO		SR0			
Description:	Load the current non-volatile NVCFG to the APC register.					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	APC					

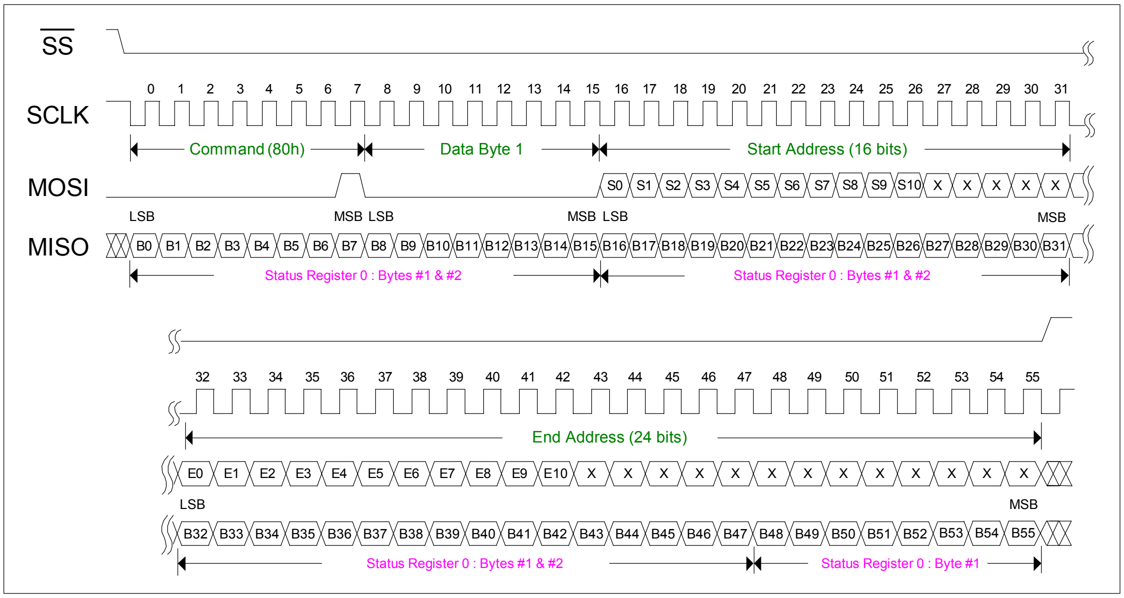
This command loads the contents of the NVCFG register into the APC register. The CMD_ERR bit of SR0 is set if ISD1700 is not in idle state when this command is sent.

11.4 DIRECT MEMORY ACCESS COMMANDS

These types of commands allow the SPI host to perform random access to any memory location by specifying the start and the end addresses. For the record and playback operations, the next pair of addresses can be preloaded. As a result, the subsequent operation jumps to the next start address seamlessly, when the operation on the first pair of addresses is finished.

All these commands require a START_ADDRESS and an END_ADDRESS. They operate from START_ADDRESS to END_ADDRESS inclusively. Because the memory is configured as a circular fashion, an END_ADDRESS smaller than START_ADDRESS is allowed. In this case, the ISD1700 will wrap around from the last row of the memory to the address 0x010 (excluding the SEs) and continue until END_ADDRESS is reached. If an END_ADDRESS is smaller than START_ADDRESS and an END_ADDRESS is also smaller than 0x10, then it will cause the device to loop endlessly, as the END_ADDRESS never matches the current address. Thus, precautions must be paid to address to the beginning of the memory. Also, care must be taken in accessing the SE rows (0x000-0x00F) and SEs should be handled independently.

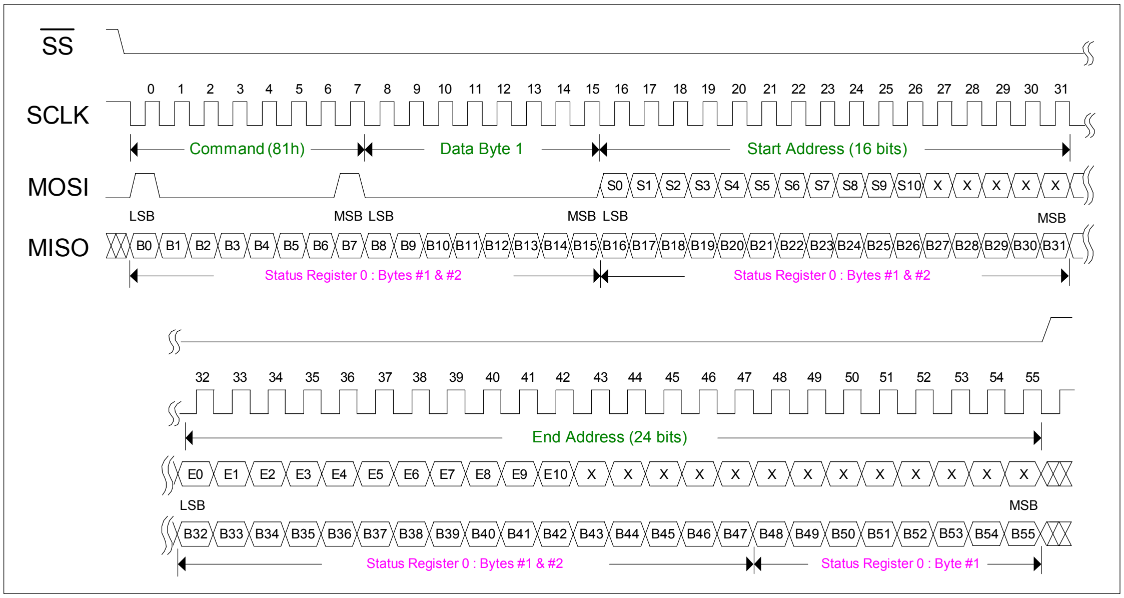
11.4.1 SET PLAY (0x80)


SS
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
Command (80h)
Data Byte 1
Start Address (16 bits)
MOSI
S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 X X X X X
LSB
MSB LSB
MSB LSB
MSB
MISO
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 B25 B26 B27 B28 B29 B30 B31
Status Register 0 : Bytes #1 & #2
Status Register 0 : Bytes #1 & #2
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
End Address (24 bits)
E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 X X X X X X X X X X X X X
LSB
MSB
B32 B33 B34 B35 B36 B37 B38 B39 B40 B41 B42 B43 B44 B45 B46 B47 B48 B49 B50 B51 B52 B53 B54 B55
Status Register 0 : Bytes #1 & #2
Status Register 0 : Byte #1

SET_PLAY	Opcode	0x80	0x00	Interrupt	Yes			
Byte Sequence:	MOSI	0x80	0x00	<S7:S0>	<00000 S10:S8>	<E7:E0>	<00000 E10:E8>	0x00
	MISO	SR0		SR0		SR0		SR0
Description:	Start a playback operation from start address <S10:S0> to end address <E10:E0> inclusive or stop at EOM, depending on the D11 of APC.							
State before Execution	Idle							
State after Execution	Idle							
Registers Affected	SR0, SR1:PLAY, RDY							

The SET_PLAY command initiates playback operation from start address <S10:S0> and stops at end address <E10:E0>. In SET_PLAY mode, the device only responds to SET_PLAY, STOP, RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR bit of SR0 is set if other commands are sent while in this mode. The RDY bit of SR1 is Low until the device has latched the addresses and begun the playback operation. If no further command is sent, the device will play until the end address <E10:E0>. Once the RDY bit of SR1 returns to High, another SET_PLAY can be sent immediately. By doing so, a second pair of START_ address and END_address is loaded into a FIFO buffer. So when the device reaches the EOM from the first end address, it doesn't stop. Instead it automatically jumps to the second start address to continue to playback operation. The purpose of executing two consecutive SET_PLAY commands is to minimize any potential dead time between two recorded messages and allow the device to concatenate two individual messages smoothly.

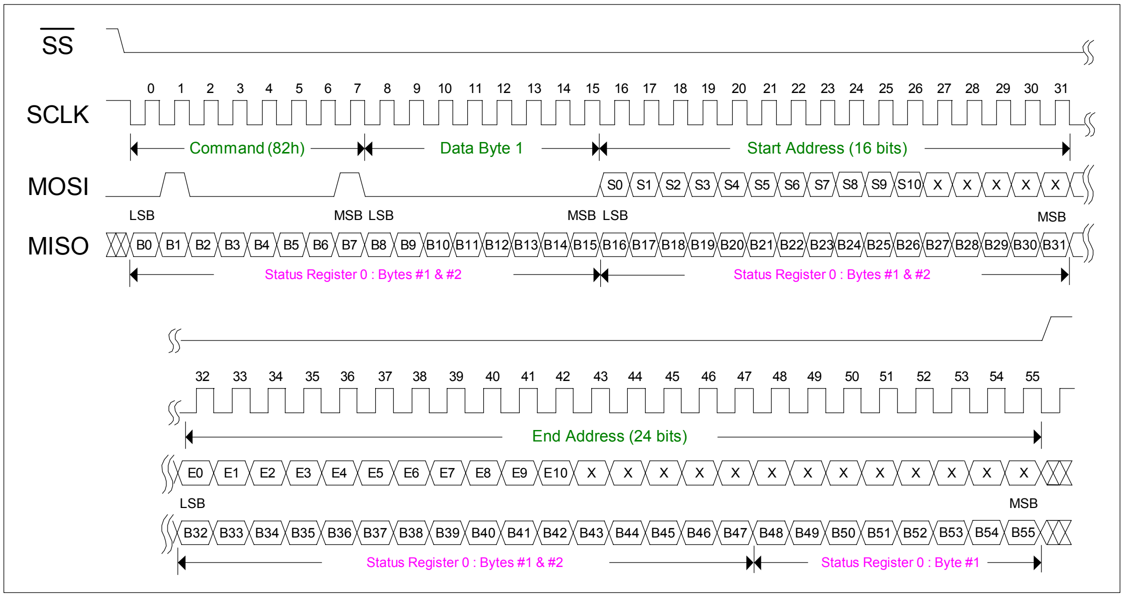
11.4.2 SET_REC (0x81)


SS
SCLK
MOSI
MISO
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
Command (81h)
Data Byte 1
Start Address (16 bits)
S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 X X X X X
LSB
MSB LSB
MSB LSB
MSB
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 B25 B26 B27 B28 B29 B30 B31
Status Register 0 : Bytes #1 & #2
Status Register 0 : Bytes #1 & #2
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
End Address (24 bits)
E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 X X X X X X X X X X X X X
LSB
MSB
B32 B33 B34 B35 B36 B37 B38 B39 B40 B41 B42 B43 B44 B45 B46 B47 B48 B49 B50 B51 B52 B53 B54 B55
Status Register 0 : Bytes #1 & #2
Status Register 0 : Byte #1

SET_REC	Opcode	0x81	0x00	Interrupt		Yes		
Byte Sequence:	MOSI	0x81	0x00	<S7:S0>	<00000 S10:S8>	<E7:E0>	<00000 E10:E8>	0x00
	MISO	SR0		SR0		SR0		SR0
Description:	Start a record operation from start address <S10:S0> to end address <E10:E0> inclusive.							
State before Execution	Idle							
State after Execution	Idle							
Registers Affected	SR0, SR1:REC, RDY							

The SET_REC command records from start address <S10:S0> and stops at end address <E10:E0>. In SET_REC mode, the device only responds to SET_REC, STOP, RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR bit of SR0 is set if other commands are sent while in this mode. The RDY bit of SR1 is Low until the device has latched addresses and begun recording. If no further command is sent, the device will record until end address <E10:E0> and write an EOM marker there. Once the RDY bit of SR1 returns to High, another SET_REC command can be sent. By doing so, a second pair of START_ address and END_address is loaded into a FIFO buffer. So when the device reaches the first end address, no EOM is written there and it automatically jumps to the second start address, then continue the recording operation. During the record process, power supply cannot be interrupted. Otherwise, it will cause the device malfunctioned.

11.4.3 SET_ERASE (0x82)


SS
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
Command (82h)
Data Byte 1
Start Address (16 bits)
MOSI
S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 X X X X X
LSB
MSB LSB
MSB LSB
MSB
MISO
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 B25 B26 B27 B28 B29 B30 B31
Status Register 0 : Bytes #1 & #2
Status Register 0 : Bytes #1 & #2
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
End Address (24 bits)
E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 X X X X X X X X X X X X X
LSB
MSB
B32 B33 B34 B35 B36 B37 B38 B39 B40 B41 B42 B43 B44 B45 B46 B47 B48 B49 B50 B51 B52 B53 B54 B55
Status Register 0 : Bytes #1 & #2
Status Register 0 : Byte #1

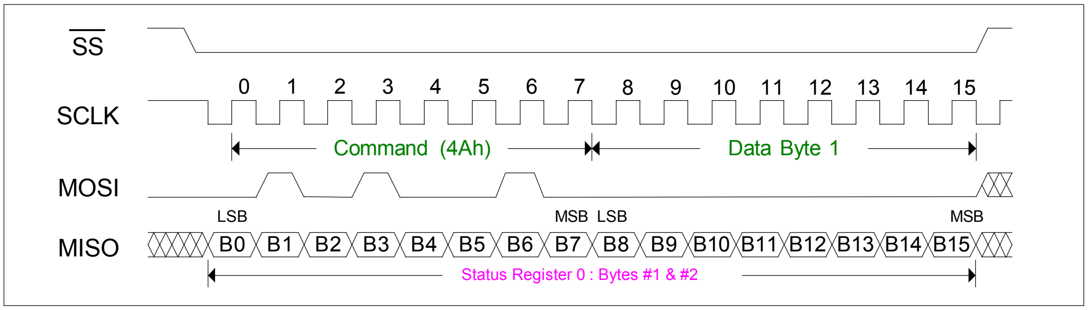
SET_ERASE	Opcode	0x82	0x00	Interrupt	Yes			
Byte Sequence:	MOSI	0x82	0x00	<S7:S0>	<00000 S10:S8>	<E7:E0>	<00000 E10:E8>	0x00
	MISO	SR0		SR0		SR0		SR0
Description:	Start an erase operation from start address <S10:S0> to end address <E10:E0> inclusive.							
State before Execution	Idle							
State after Execution	Idle							
Registers Affected	SR0, SR1:ERASE, RDY							

The SET_ERASE command erases rows from start address <S10:S0> to end address <E10:E0> inclusively. In this mode, the device will only respond to RESET, CLR_INT, RD_STATUS and PD commands. The CMD_ERR bit of SR0 is set when other commands are sent. The RDY bit of SR1 is Low until erasure is completed and an interrupt is generated. During the erase process, power supply cannot be interrupted. Otherwise, it will cause the device malfunctioned.

11.5 Additional Command

The additional command enhances the functionality and performance of the device in order to fulfill extra features and requirements that the designers may wish.

11.5.1 EXTCLK (0x4A)



EXTCLK	Opcode	0x4A	0x00	Interrupt	No	
Byte Sequence:	MOSI	0x4A	0x00			
	MISO	SR0				
Description:	Enable or disable the external clock mode					
State before Execution	Idle					
State after Execution	Idle					
Registers Affected	None					

The EXTCLK command toggles the enable and disable of the external clock (XCLK) mode on the device. When XCLK mode is activated, the internal oscillator of the device is disabled. Instead, an external clock is required to apply to the Rosc pin and the external resistor at Rosc pin must be removed. When XCLK mode is disabled, then the external clock signal must be disconnected from Rosc pin and an external resistor must be connected back, so that the device runs from its internal clock accordingly. This mode is very useful for synchronization of the I1700 device with an external component, such as microcontroller, when precision timing is essential. An active XCLK state can also be reset by RESET command or RESET pin. Hence, the device will operate via its internal oscillator, provided that the external resistor is hooked up to the Rosc pin.

The frequencies of the required external clock with respect to the various sampling frequencies are listed in the below table, but duty cycle is not important since it will be taken care internally by the device.

Sampling Freq. [kHz]	12	8	6.4	5.3	4
External Clock Freq. [MHz]	3.072	2.048	1.638	1.356	1.024

11.6 GENERAL GUIDELINES FOR WRITING PROGRAM CODE

Besides realizing the basic functions under Standalone mode (if not, one should study the contents of Section 8), the software engineers must also fully understand the definition of each SPI command and how to implement each of them correctly (if not, one should review and comprehend the contents from Section 10 through Section 11.5). Then the next move is how to link up the operating codes together and perfectly, so that the program runs smoothly. The following rules, but not limited to, should be applied.

Rule #1: "*Is the command just sent being accepted and executed correctly*?" In order to validate this, one has to ensure that:

(a) Is the device ready to accept the new instruction?

Solution : Before any new instruction is sent, one can query the device's ready status and confirm that from either the RDY bit of SR1 or the $\mathrm{RDY}/\overline{\mathrm{INT}}$ pin.

(b) Is the prior command sent being accepted?

Solution : One can check and confirm whether the CMD_ERR bit of SR0 is set (=1) or not after the instruction code is sent.

All these can be achieved by utilizing the RD_STATUS command.

Rule #2: After the newly instruction code is accepted and executed, one needs to know "*Does the operation function as expected?*" The LED indication associated with certain operations in Standalone mode is not automatically embedded in the SPI similar functions. Hence, enabling the LED feature (bit C4) on all the operations is a good habit because this will provide a direct visual illustration to the end user, such as LED on during recording or LED blinking during playback, if LED is connected appropriately, and etc.

Rule #3: While an operation is in progress, one needs to know "*When the current operation completes*". So that the next instruction code can be sent immediately to make the best use of the microcontroller's time and efficiency. This requires a feedback from ISD1700 device and can be achieved by monitoring the status change on either the INT bit of SR0 or the $\mathrm{RDY}/\overline{\mathrm{INT}}$ pin.

Rule #4: One must also be conscious about the characteristics of the interrupt. Once an interrupt is set, its status remains unaltered until it is cleared. The only way to clear an interrupt is to issue a CLR_INT command. In order to avoid any confusion on monitoring the interrupt status of consecutive instruction codes, one must immediately clear the interrupt set by the just-finished operation before the next instruction code is sent.

Rule #5: As mentioned earlier, some commands (14 out of 24) have no interference on the interrupt status. These commands are:

- PU, PD, RESET, CLR_INT, RD_STATUS, DEV_ID,
- RD_APC, WR_APC1, WR_APC2, WR_NVCFG, LD_NVCFG,
- RD_PLAY_PTR, RD_REC_PTR, EXTCLK

Since most of these commands perform inquiries from the device or changing the internal setting within the device, some people may think the device would perform the task fairly quick. Thus, a common mistake will occur that two consecutive command codes are submitted without checking whether the device is ready to accept the next command (as

Rule #1) or inserting an appropriate delay between the codes. As a result, the 2nd command will be ignored. Bear in mind that no matter how quick the related task in ISD1700 can be performed, but its speed is still slower than that of code transmission from microcontroller.

Therefore, after any of these commands is issued, one need to monitor the status on either the RDY bit of SR1 or the $\mathrm{RDY}/\overline{\mathrm{INT}}$ pin to guarantee that the device is in Ready mode prior to a new instruction being sent. Otherwise, the new instruction will be omitted.

Nevertheless, some programmers may prefer to insert a delay between two instruction codes for simplicity, rather than to monitor the Ready status. If that's the case, one must insert a "sufficient" delay between the instruction codes. With a "sufficient" delay provided, one then can guarantee that the next instruction code will be successfully accepted after the execution on the current operation completes. Remember the frequency that the ISD1700 operates is pending upon an external resistor (typically, the common used ones have +/-5% or +/-10% accuracy for cost reason). Another precaution is that microcontrollers run code in μsec, but the ISD1700 completes a task in msec. Since the time for ISD1700 to accomplish a task is a variable factor pending upon the type of task, sampling frequency and other external factors, one may need to do the trial and error experiments in order to search for an optimum number. For example, with 8kHz sampling frequency, one can use 100 msec as a starting point, then adjust back and forth to search for that number. Due to the uncontrollable external factors, the approach of utilizing delay is not recommended, unless additional buffer on the delay is factored in.

Rule #6: Set initial SPI condition as listed in Section 10.2 before any SPI command is sent.

Rule #7: To access the sound effects, one needs to use Set commands. The debounce time needed for certain operation in Standalone mode is not required in SPI mode.

11.7 EXAMPLES OF VARIOUS OPERATING SEQUENCES

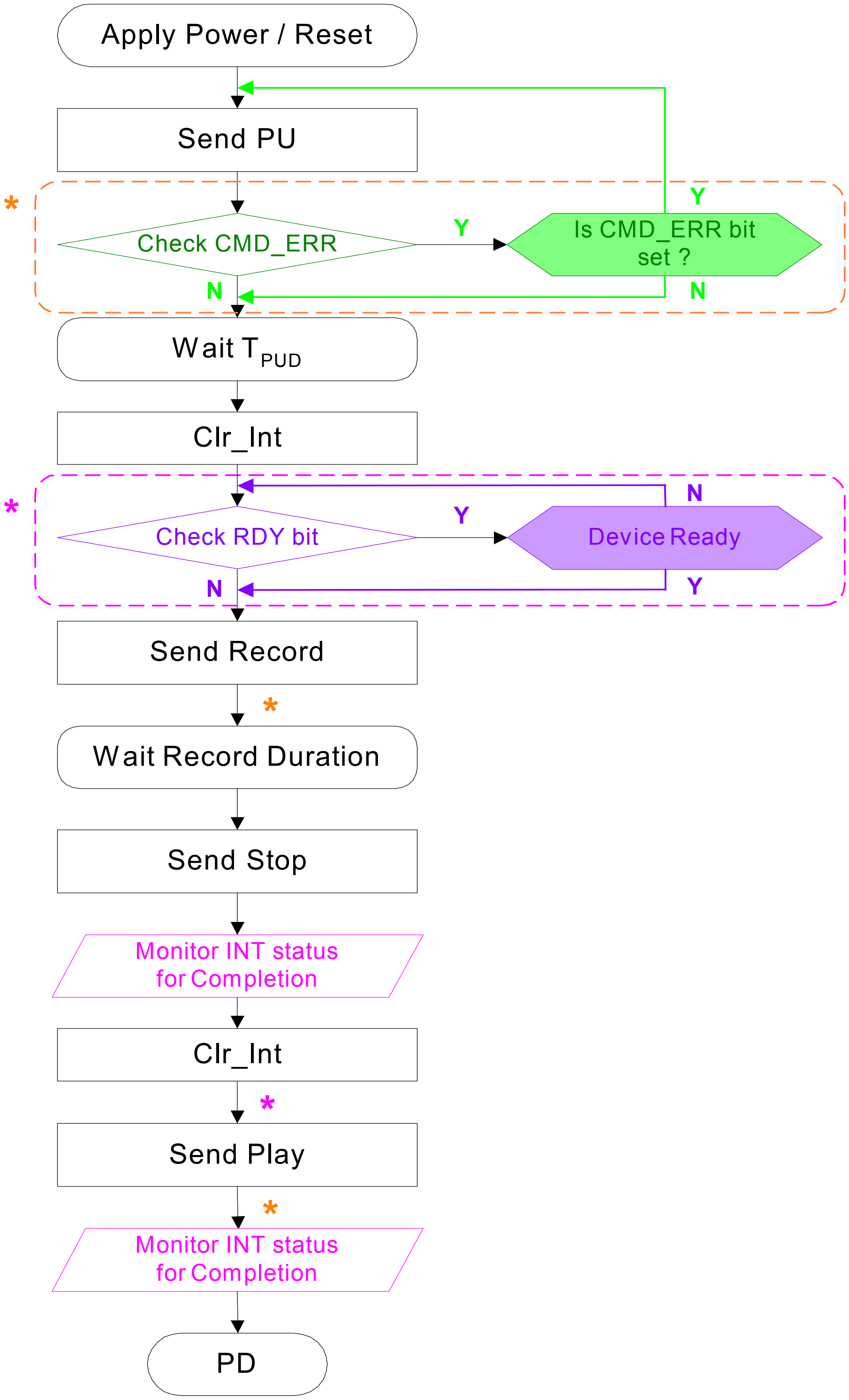
The following flow chart examples illustrate various generic approaches on certain types of operating sequences. The flow charts review the typical required steps among different kinds of operations. The objective is to ensure each desired operation is performed as expected without any omission. These examples merely serve as references for writing program codes and make no representation that they are guaranteed to be functional at any systems flawlessly. Its software engineers' responsibility to debug their own program code faultlessly in their system designed according to the applications. The operating sequences on the ISD1700 devices are not limited to those as shown.

The following example sequences are mainly to demonstrate:

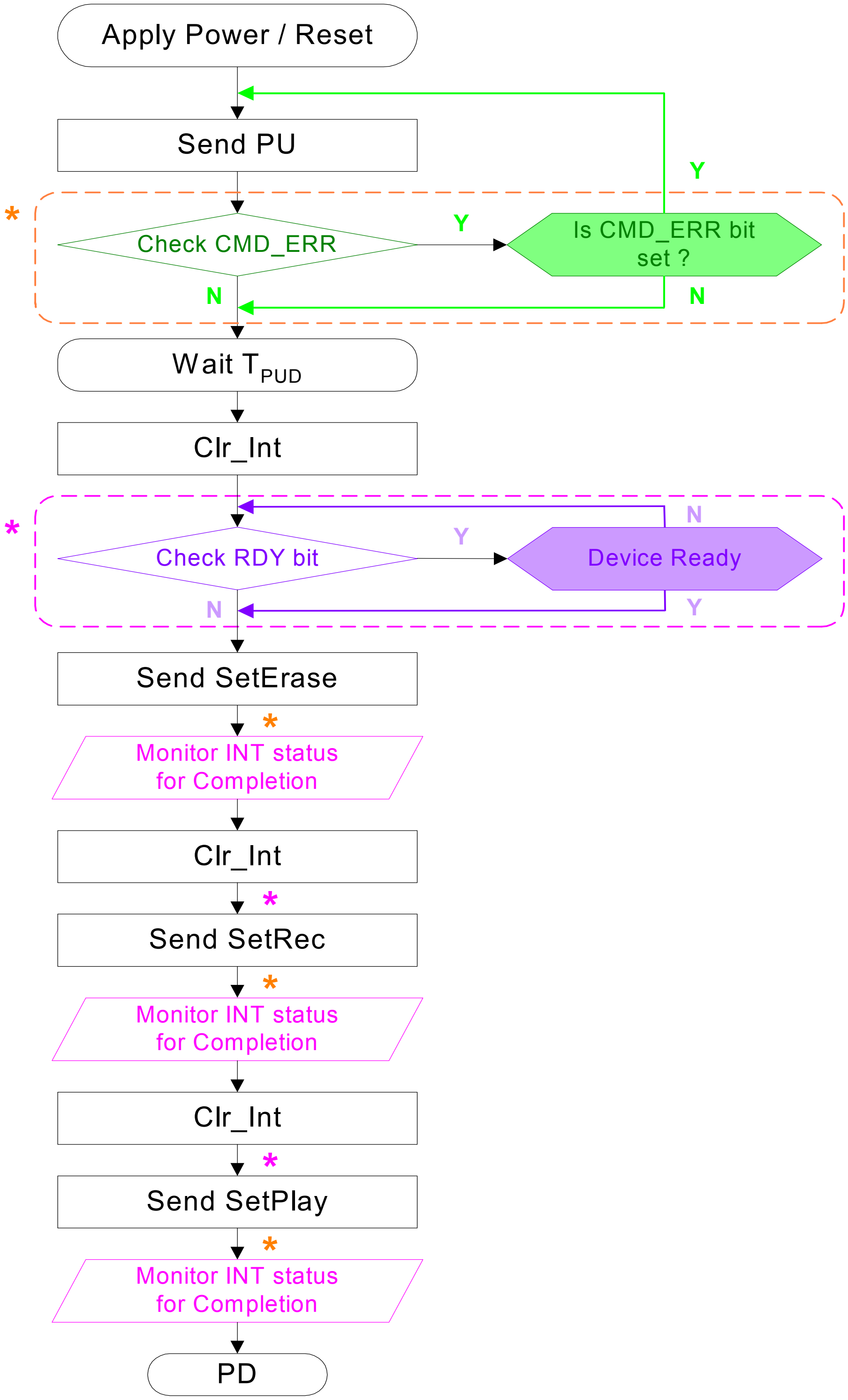
- Record, Stop and Playback sequence.
- SetErase, SetRec and SetPlay sequence.
- Wr_APC2, SetRec and SetPlay sequence.
- Playback 3 messages as 1 message sequence.

Once the programmers get familiar with the methodology, they can apply the similar techniques on the related SPI commands and generate their own sequences with respect to the applications required. These examples offer a number of advantages, ultimately resulting in less effort and resources spending on programming, providing a viable path for code development in an effective and efficient way.

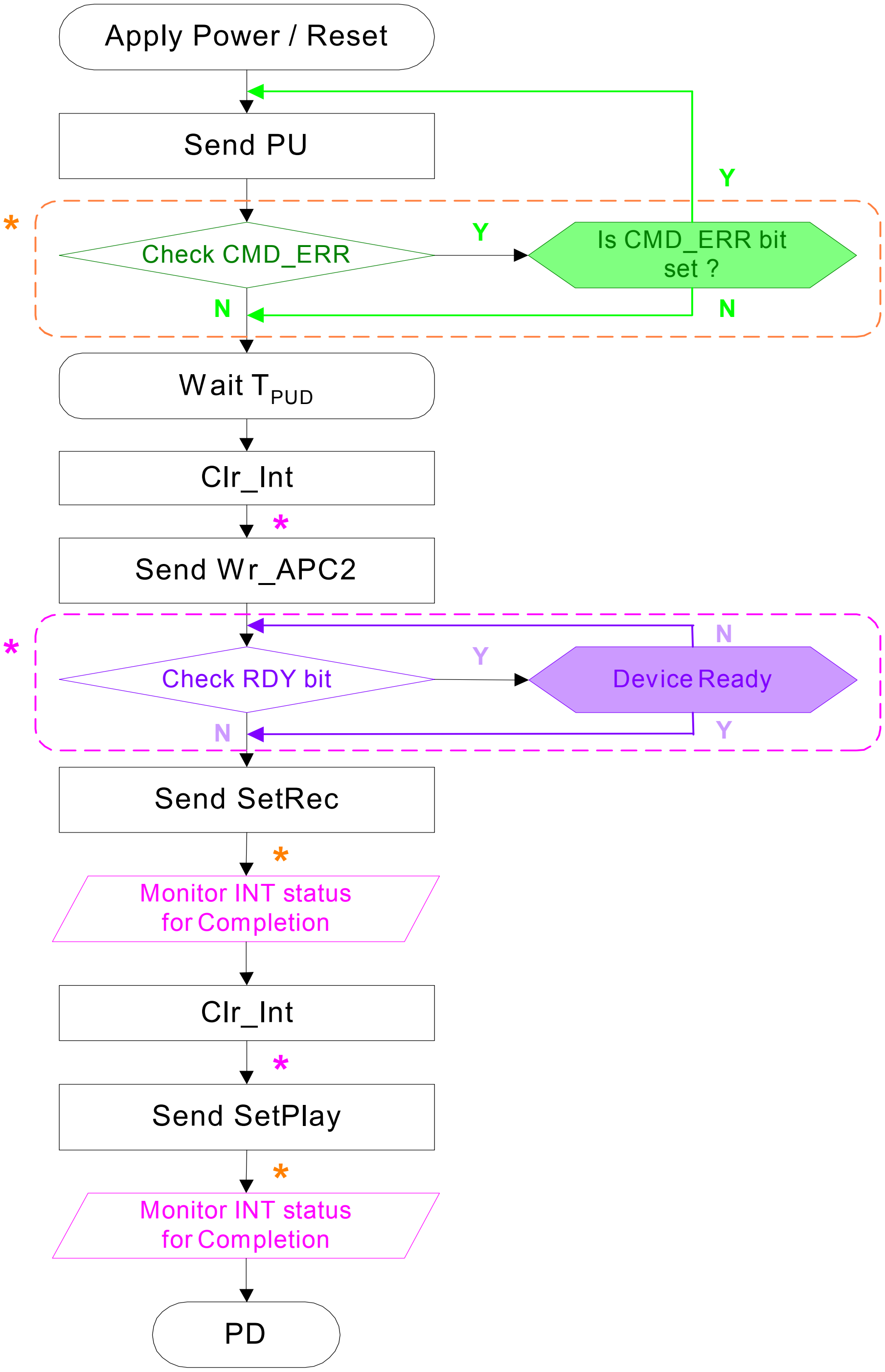
11.7.1 Record, Stop and Playback operations



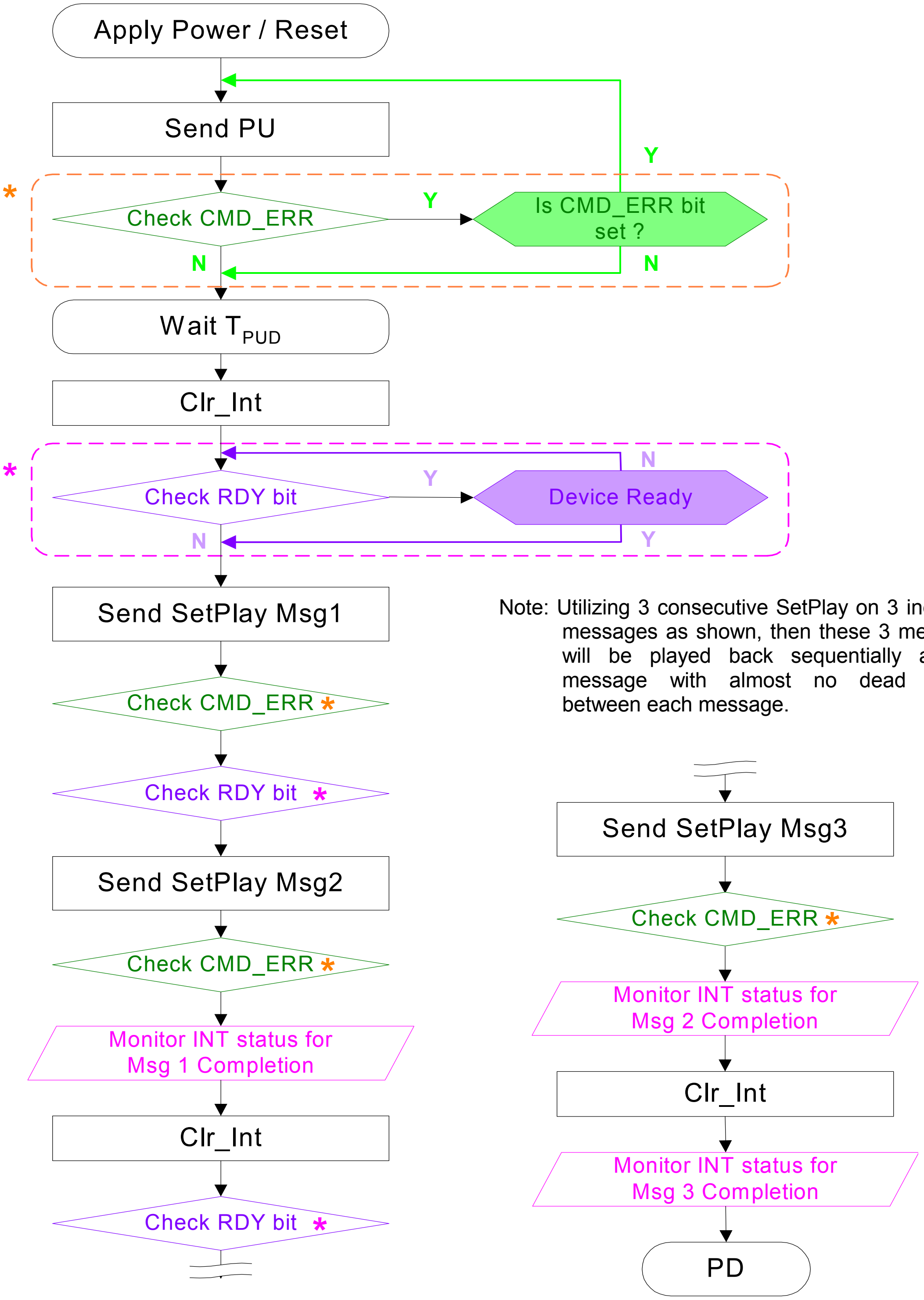
11.7.2 SetRec and SetPlay operations



11.7.3 Wr_APC2, SetRec and SetPlay operations



11.7.4 Playback 3 Messages as 1 Message (using SetPlay)



Note: Utilizing 3 consecutive SetPlay on 3 individual messages as shown, then these 3 messages will be played back sequentially as one message with almost no dead silence between each message.

12 TIMING DIAGRAMS

The following estimated timing diagrams are for basic operation and are not in proper scale. The LED and optional SE indications include automatically in certain operations under Standalone mode, but not under the SPI mode.

12.1 RECORD OPERATION

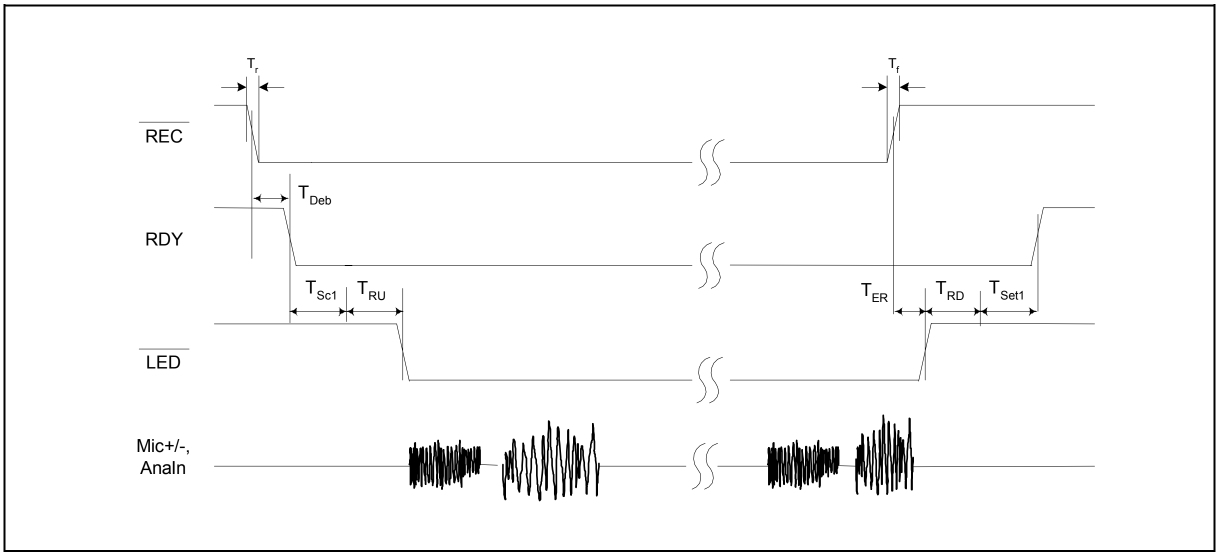


Figure 12.1: Record Operation with No Sound Effect

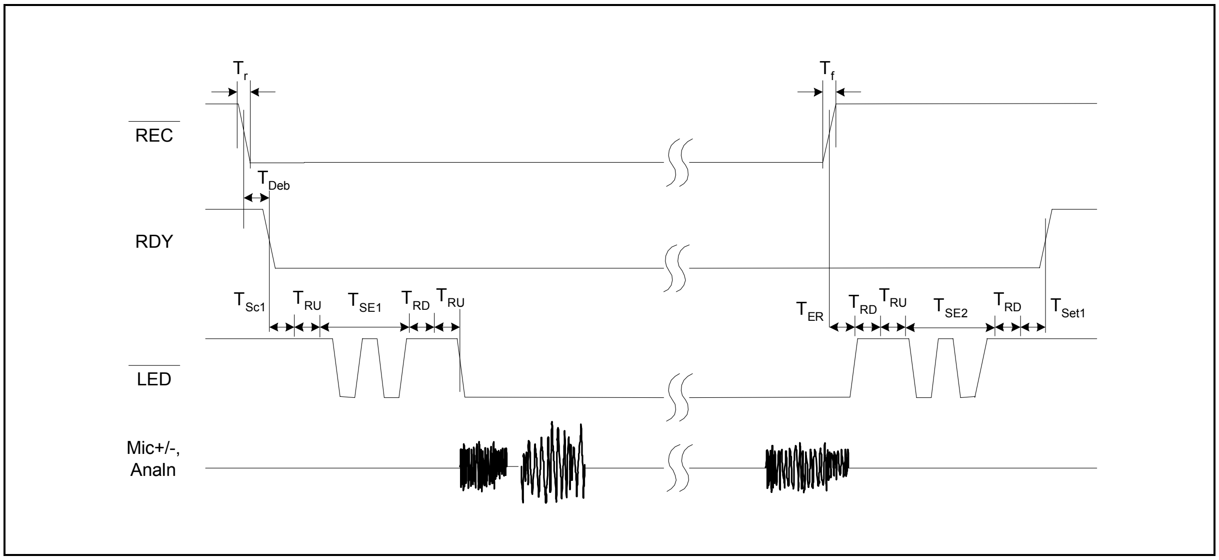


Figure 12.2: Record Operation with Sound Effect

12.2 PLAYBACK OPERATION

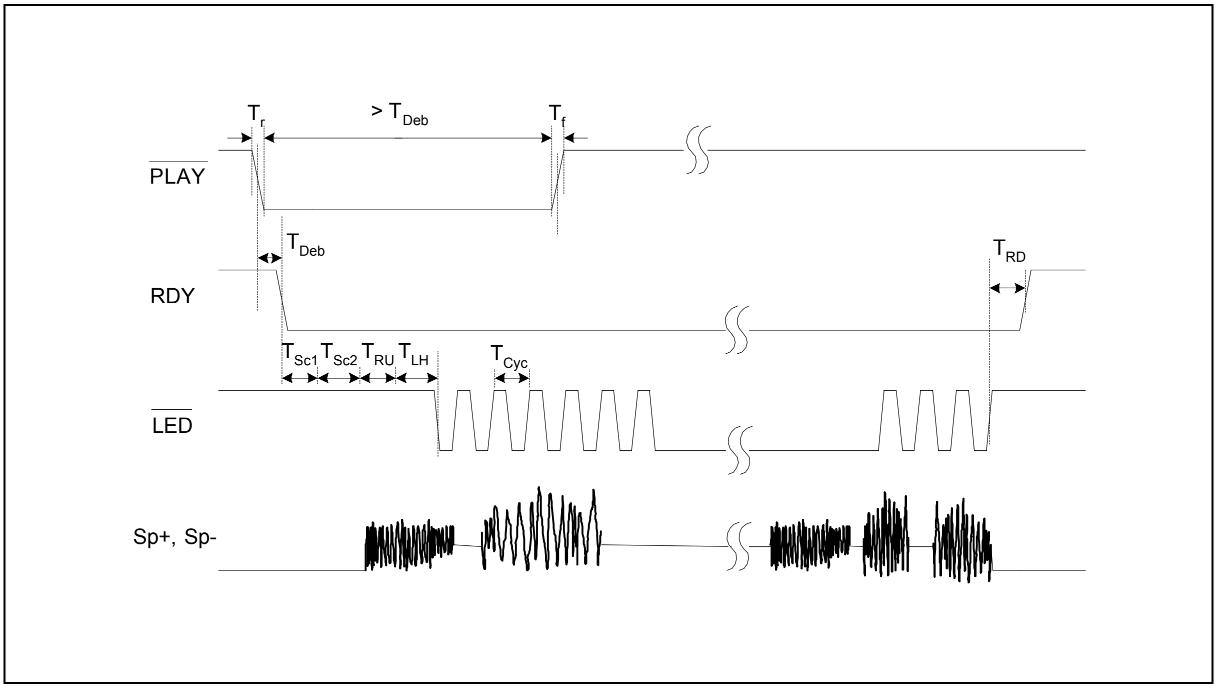


Figure 12.3: Playback Operation for entire message

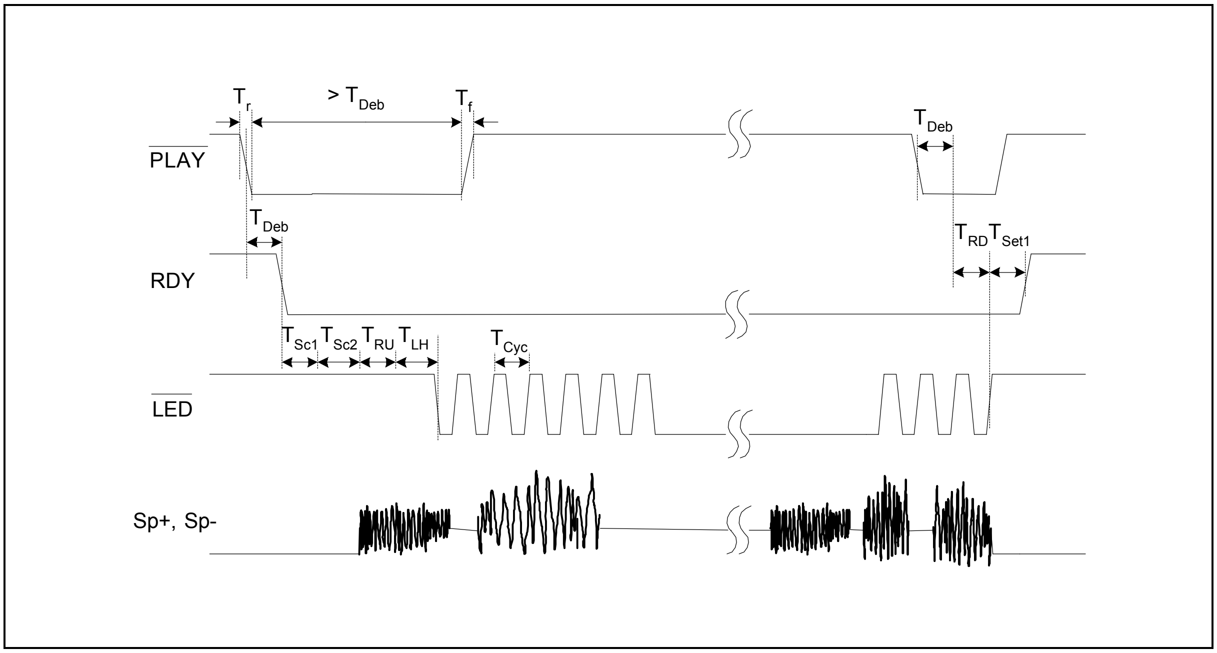


Figure 12.4: Start and Stop Playback Operation

12.3 Erase Operation

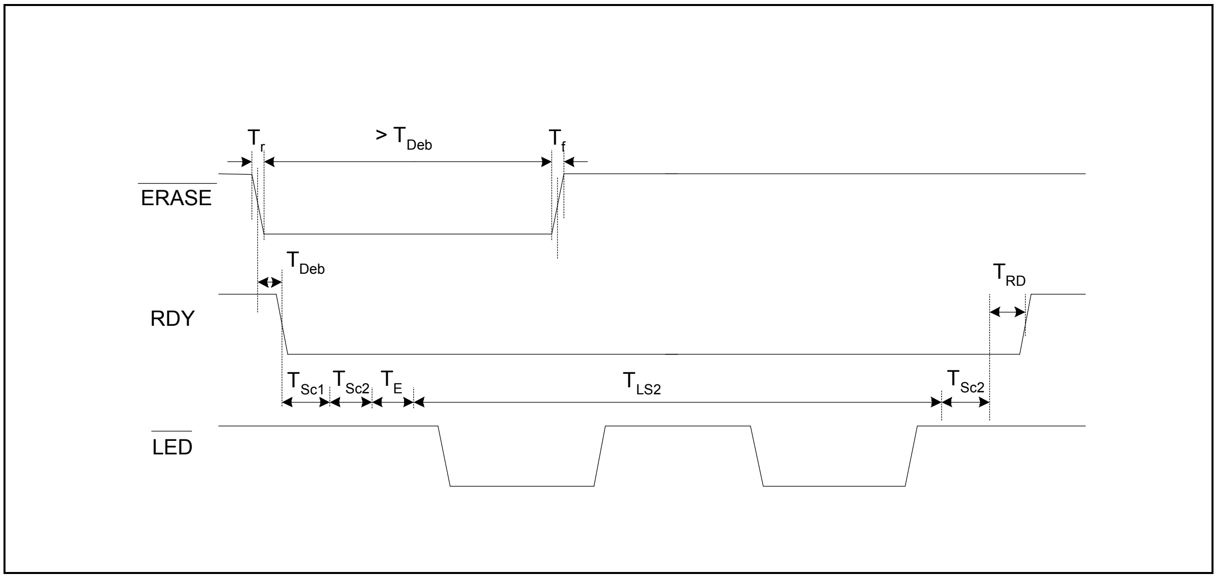


Figure 12.5: Single Erase Operation with No Sound Effect

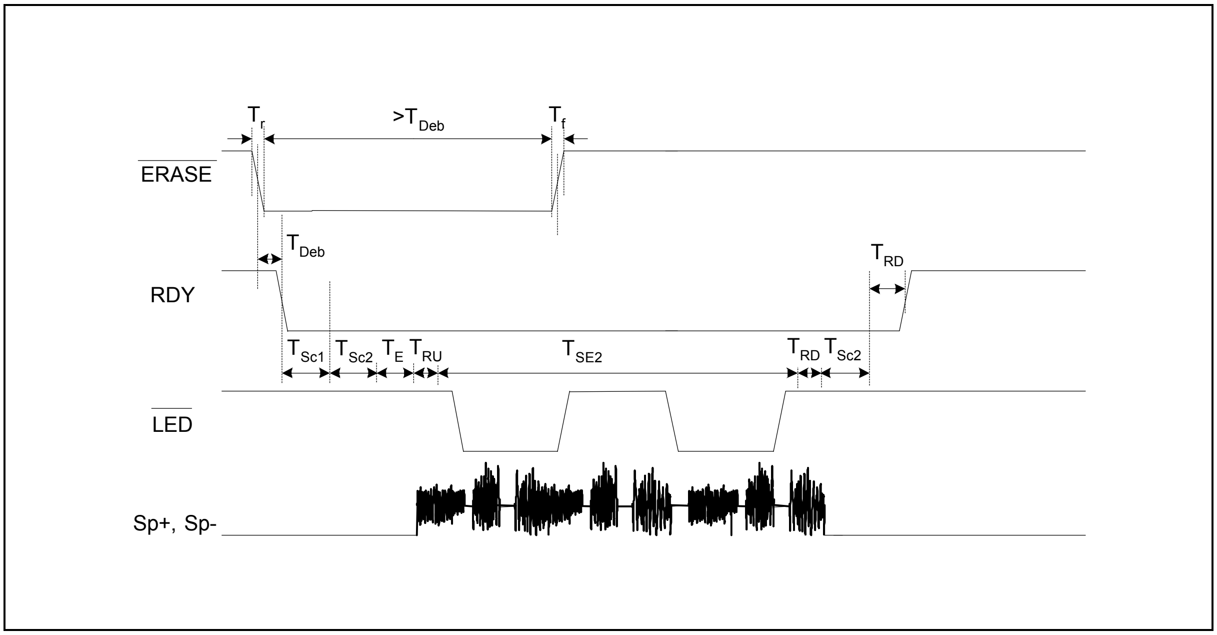


Figure 12.6: Single Erase Operation with Sound Effect

12.4 FORWARD OPERATION

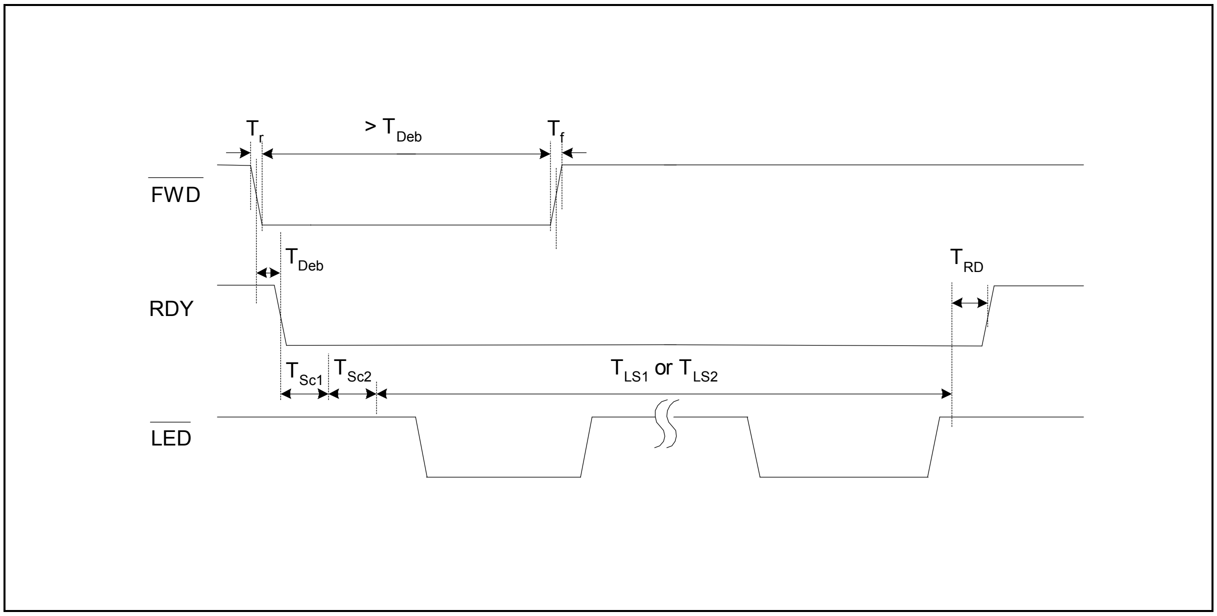


Figure 12.7: Forward Operation with No Sound Effect

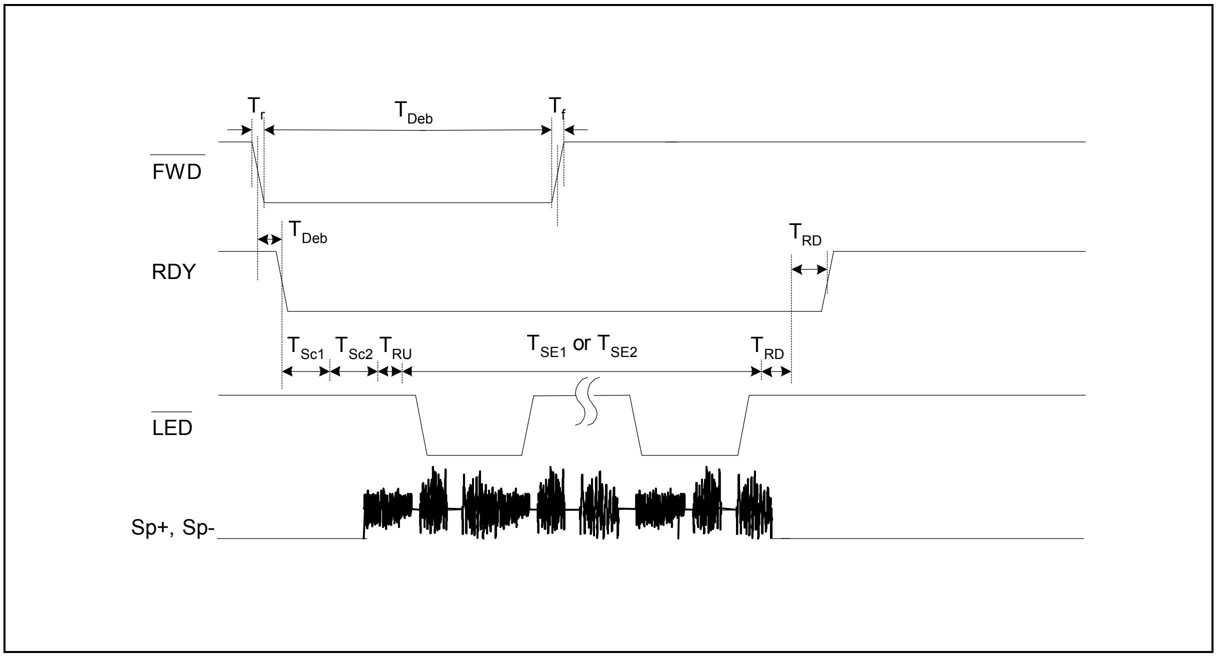


Figure 12.8: Forward Operation with Sound Effect

12.5 GLOBAL ERASE OPERATION

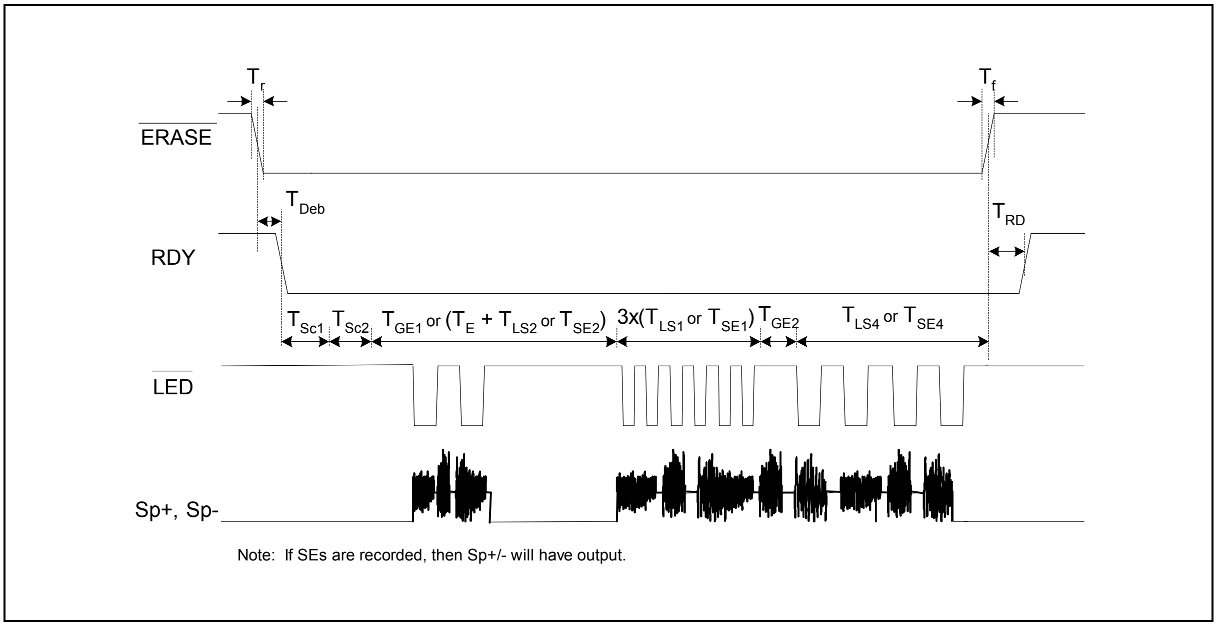

T_r
T_f
$\overline{ERASE}$
T_{Deb}
T_{RD}
RDY
T_{Sc1} T_{Sc2} T_{GE1} or (T_E + T_{LS2} or T_{SE2}) 3x(T_{LS1} or T_{SE1}) T_{GE2} T_{LS4} or T_{SE4}
$\overline{LED}$
Sp+, Sp-
Note: If SEs are recorded, then Sp+/- will have output.

Figure 12.9: Global Erase Operation with or without Sound Effects

12.6 RESET OPERATION

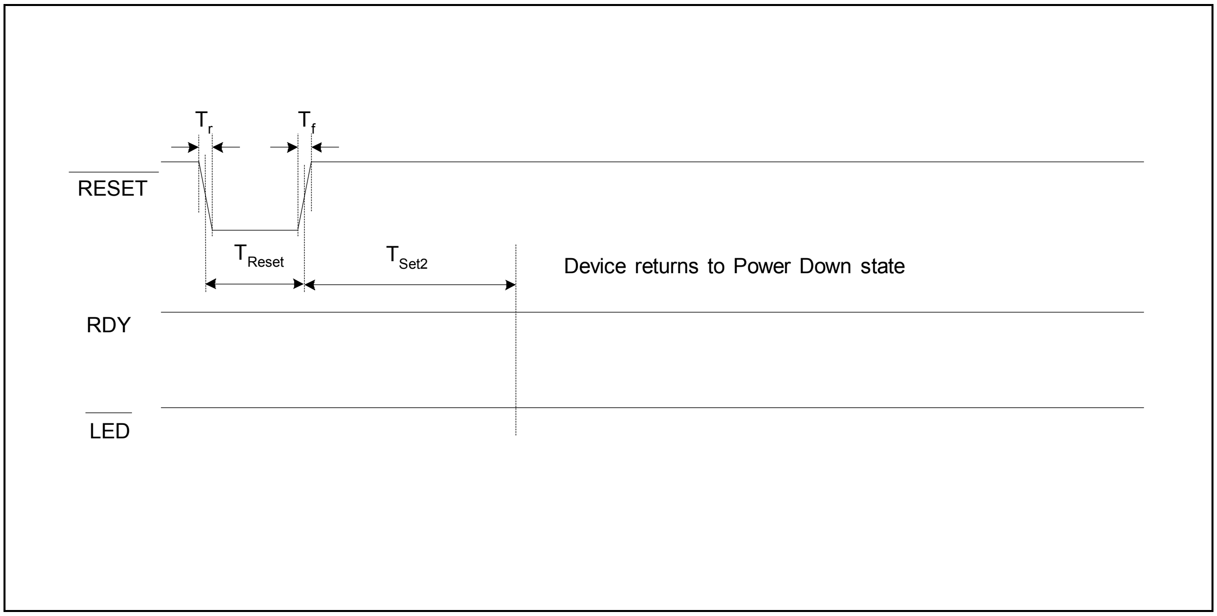


Figure 12.10: Reset Operation

12.7 LOOPING PLAYBACK OPERATION

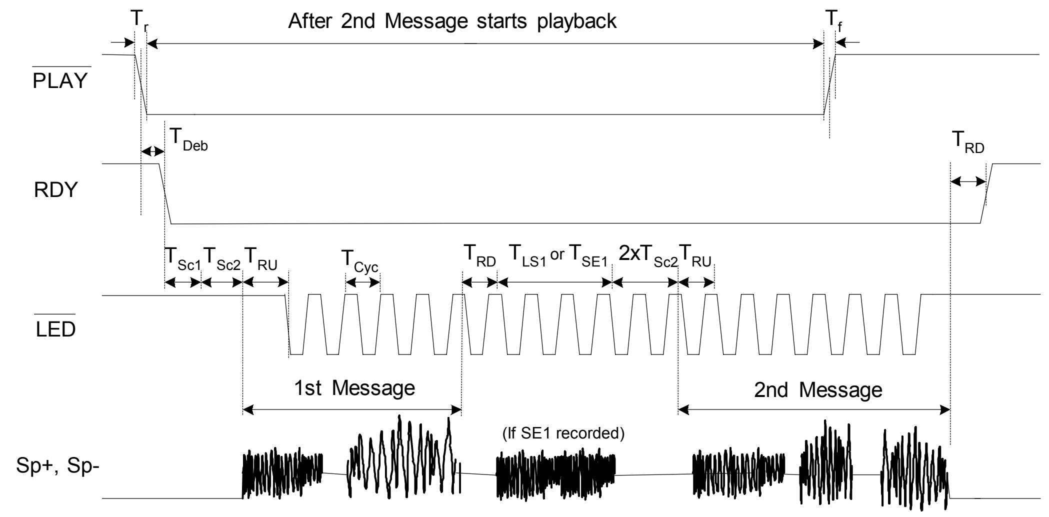


Figure 12.11: Playback Two Consecutive messages

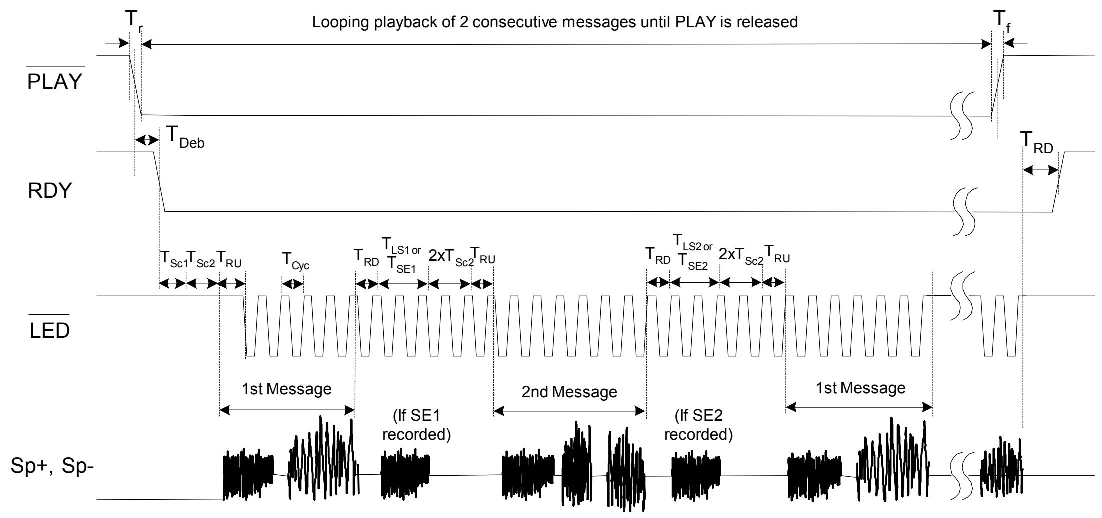

T_r
Looping playback of 2 consecutive messages until PLAY is released
T_f
$\overline{PLAY}$
T_{Deb}
T_{RD}
RDY
T_{Sc1} T_{Sc2} T_{RU}
T_{Cyc}
T_{RD} T_{LS1} or T_{SE1} $2xT_{Sc2}$ T_{RU}
T_{RD} T_{LS2} or T_{SE2} $2xT_{Sc2}$ T_{RU}
$\overline{LED}$
1st Message
(If SE1 recorded)
2nd Message
(If SE2 recorded)
1st Message
Sp+, Sp-

Figure 12.12: Looping Playback with Two messages

12.8 GLOBAL ERASE OPERATION TO RESTORE CIRCULAR MEMORY ARCHITECTURE

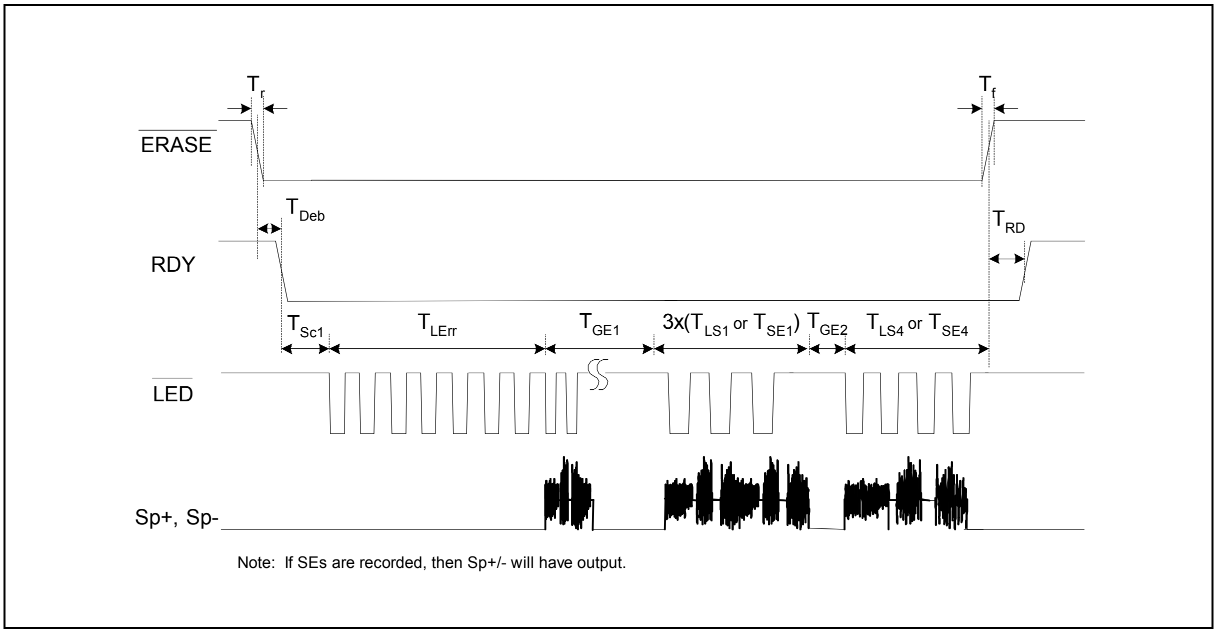


Figure 12.13: Global Erase Operation to recover a broken circular memory architecture

12.9 PLAYBACK OPERATION WITH AUD OUTPUT

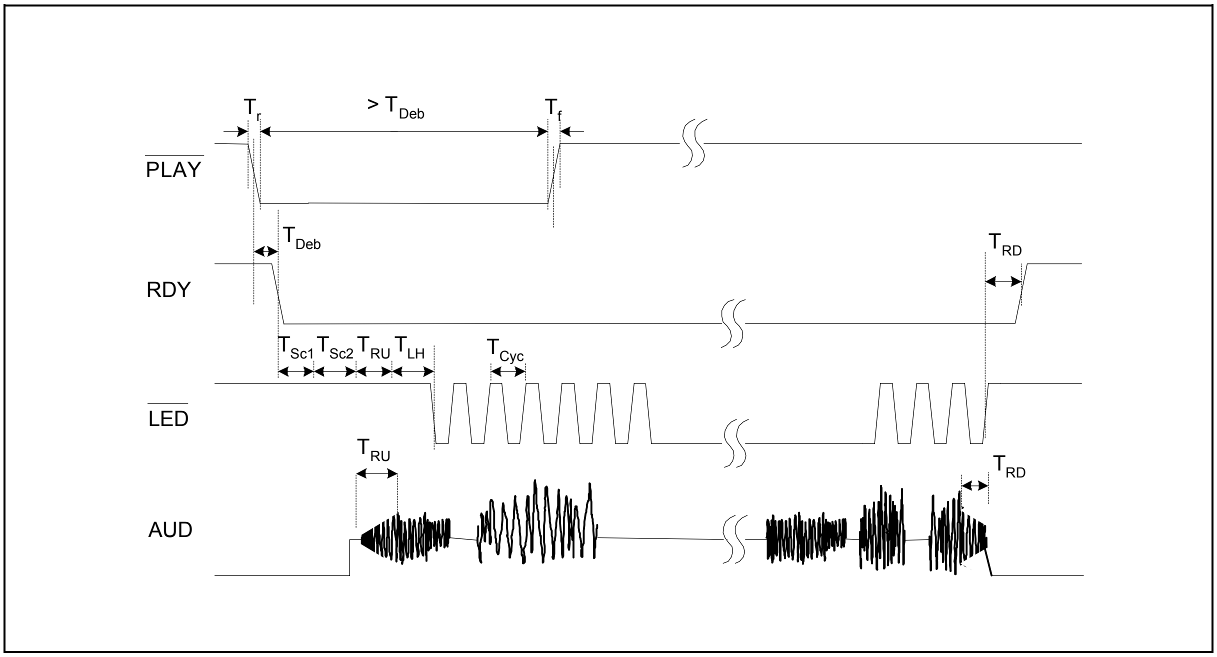


Figure 12.14: Playback Operation with ramp up and ramp down effect at AUD output

12.10 SPI OPERATION

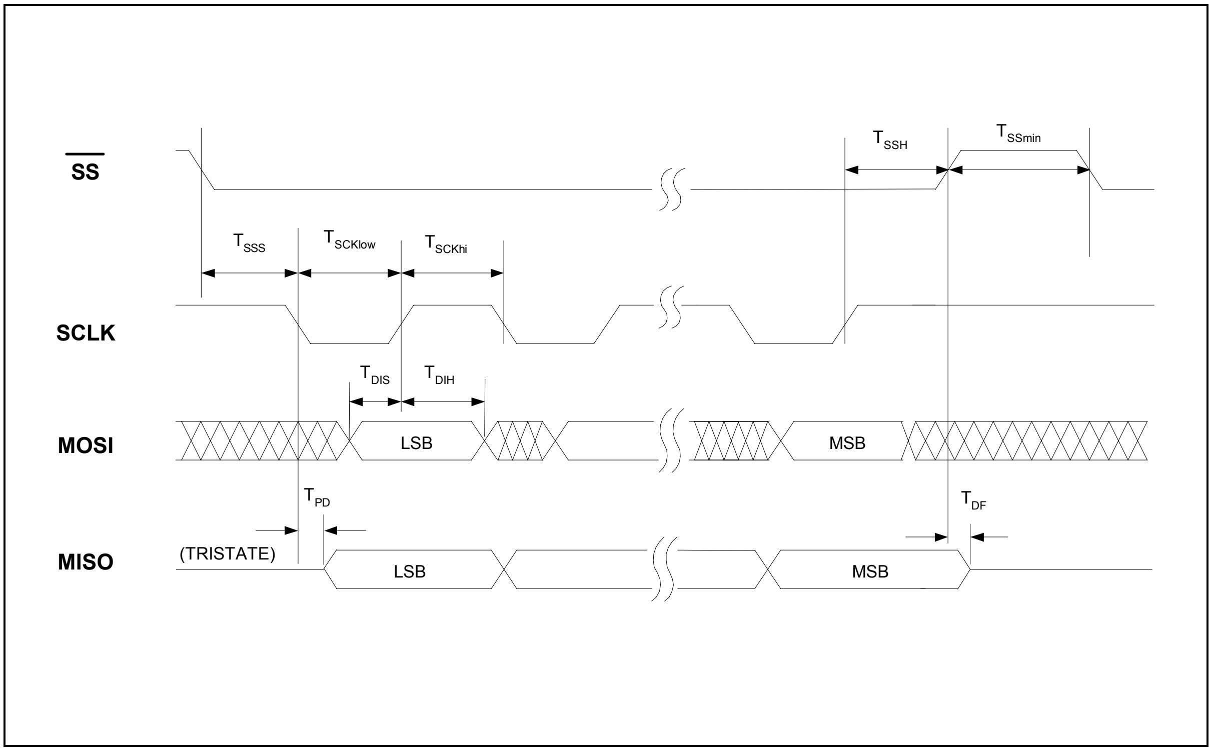


Figure 12.15: SPI Operation

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
$\overline{SS}$ Setup Time	T_{SSS}	500			nsec
$\overline{SS}$ Hold Time	T_{SSH}	500			nsec
Data in Setup Time	T_{DIS}	200			nsec
Data in Hold Time	T_{DIH}	200			nsec
Output Delay	T_{PD}			500	nsec
Output Delay to HighZ	T_{DF}			500	nsec
$\overline{SS}$ HIGH	T_{SSmin}	1			µsec
SCLK High Time	T_{SCKhi}	400			nsec
SCLK Low Time	T_{SCKlow}	400			nsec
CLK Frequency	F_0			1,000	KHz
Power-Up Delay [1]	T_{PUD}		50		msec

Notes: [1] Timing parameter given is based upon 8 kHz sampling freq and varied according to sampling freq.

13 ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (DIE) [1]

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pads	(V_{SS} - 0.3V) to (V_{CC} + 0.3V)
Power supply voltage to ground potential	-0.3V to +7.0V

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS) [1]

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pins	(V_{SS} - 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Power supply voltage to ground potential	-0.3V to +7.0V

[1] *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

13.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+2.4 V to +5.5 V
Ground voltage (V_{SS}) [2]	0 V
Input voltage (V_{CC}) [1]	0 V to 5.5 V
Voltage applied to any pins	(V_{SS} –0.3 V) to (V_{CC} +0.3 V)

OPERATING CONDITIONS (PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Supply voltage (V_{DD}) [1]	+2.4V to +5.5V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 5.5V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

[1] $V_{CC} = V_{CCA} = V_{CCD} = V_{CCP}$

[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSP1}\ V_{SSP2}$

14 ELECTRICAL CHARACTERISTICS

14.1 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.4		5.5	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 4.0 mA[2]
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1.6 mA[2]
Record Current	I_{DD_Record}		20		mA	V_{DD} = 5.5 V, No load, Sampling freq = 12 kHz
Playback Current	$I_{DD\_Playback}$		20		mA	
Erase Current	I_{DD_Erase}		20		mA	
Standby Current	I_{SB}		0.5	1	µA	V_{DD} = 5.5 V, T=25°C [3] [4]
Input Leakage Current	I_{ILPD1}			±1	µA	Force V_{DD}
Input Current Low	I_{ILPD2}	-3		-10	µA	Force V_{SS} , others at Vcc
Preamp Input Impedance	R_{MIC+},R_{MIC-}		7		kΩ	Power-up AGC
AnaIn Input Impedance	R_{AnaIn}		42		kΩ	When active
MIC Differential Input	V_{IN1}	15		300	mV	Peak-to-Peak[5]
AnaIn Input Voltage	V_{IN2}			1	V	Peak-to-Peak
Gain from MIC to SP+/-	A_{MSP}	6		40	dB	V_{IN} = 15~300 mV, AGC = 4.7 µF, V_{CC} = 2.4V~5.5V
Speaker Output Load	R_{SPK}	8			Ω	Across both Speaker pins
AUX Output Load	R_{Aux}	5			kΩ	When active
Speaker Output Power	Pout		670		mW	V_{DD} = 5.5 V 1Vp-p, 1 kHz sine wave at AnaIn. R_{SPK} = 8 Ω.
			313		mW	V_{DD} = 4.4 V
			117		mW	V_{DD}= 3 V
			49		mW	V_{DD}= 2.4 V
Speaker Output Voltage	V_{OUT1}		V_{DD}		V	R_{SPK} = 8Ω (Speaker), Typical buzzer
AUX Output Swing	V_{OUT2}			1	V	Peak-to-Peak
AUX Output DC Level	V_{OUT3}		1.2		V	When active
AUD	I_{AUD}		-3.0		mA	V_{DD} =4.5 V, R_{EXT}= 390 Ω
Volume Output	A_{Vol}		0 to -28		dB	8 steps of 4dB each reference to output
Total Harmonic Distortion	THD		1		%	15 mV p-p 1 kHz sine wave, Cmessage weighted

Notes:
[1] Conditions: V_{CC} = 4.5V, 8 kHz sampling frequency and T_A = 25°C, unless otherwise stated.
[2] LED output during Record operation.
[3] V_{CCA}, V_{CCD} and V_{CCP} are connected together. V_{SSA}, V_{SSP1}, V_{SSP2} and V_{SSD} are connected together.
[4] $\overline{\textbf{REC}}$, $\overline{\textbf{PLAY}}$, $\overline{\textbf{FT}}$, $\overline{\textbf{FWD}}$, $\overline{\textbf{ERASE}}$, $\overline{\textbf{VOL}}$ and $\overline{\textbf{RESET}}$ must be at V_{CCD}.
[5] Balanced input signal applied between MIC+ and MIC- as shown in the applications example. Single-ended MIC+ or MIC- input is recommended no more than 150 mV p-p.

14.2 AC PARAMETERS

CHARACTERISTIC	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Sampling Frequency [2]	F_S	4		12	kHz	[4]
Duration [3]	T_{Dur}		Sect. 6.1.2		sec	
Rising Time	T_r			100	nsec	
Falling Time	T_f			100	nsec	
Debounce Time	T_{Deb}	$192/F_S$			msec	[4] [6]
Ramp Up Time	T_{RU}		$128/F_S$		msec	
Ramp Down Time	T_{RD}		$128/F_S$		msec	
Initial Scan Time after power is applied	T_{Sc1}			$DRN/8/F_S$	msec	DRN= device row# [4]
Initial Scan Time from PD state	T_{Sc2}			$DRN/16/F_S$	msec	After a PB operation is run [4]
End Recording Time	T_{ER}			$32/F_S$	msec	[4]
LED High Time	T_{LH}			$0.5K/F_S$	msec	[4]
LED Flash Time for SE1	T_{LS1}		$3.5K/F_S$		sec	SE1 not recorded [5]
LED Flash Time for SE2	T_{LS2}		$7.5K/F_S$		sec	SE2 not recorded [5]
LED Flash Time for SE3	T_{LS3}		$11.5K/F_S$		sec	SE3 not recorded [5]
LED Flash Time for SE4	T_{LS4}		$15.5K/F_S$		sec	SE4 not recorded [5]
SE1 Recorded Duration	T_{SE1}			$4K/F_S$	sec	[4] [5]
SE2 Recorded Duration	T_{SE2}			$4K/F_S$	sec	[4] [5]
SE3 Recorded Duration	T_{SE3}			$4K/F_S$	sec	[4] [5]
SE4 Recorded Duration	T_{SE4}			$4K/F_S$	sec	[4] [5]
Erase Time	T_E		$10MRN/F_S$		sec	MRN=message row # [4]
Global Erase Wait Time	T_{GE1}			$20K/F_S$	sec	[4] [5]
Global Erase Time	T_{GE2}		$34/F_S$		sec	
RESET Pulse	T_{Reset}	1			µsec	All Fs [4]
Settle Time	T_{Set1}			$128/F_S$	msec	[4]
Settle Time after Reset	T_{Set2}			$64/F_S$	msec	[4]
LED Error Time	T_{LErr}			$27.5K/F_S$	msec	[4] [5]
LED Cycle frequency	T_{Cyc}	1		4	Hz	Pending upon F_S

Notes: [1] Typical values: V_{CC} = 4.5 V, F_S = 8 kHz and @ T_A = 25°C, unless otherwise stated.

[2] Characterization data shows that sampling frequency resolution is ±5 percent across temperature and voltage ranges.

[3] Characterization data shows that duration resolution is ±5 percent across temperature and voltage ranges.

[4] Vcc=2.4 V~5.5V

[5] K = 1024

[6] Debounce time is only applicable to operations in standalone mode and is not applicable to the related SPI commands.

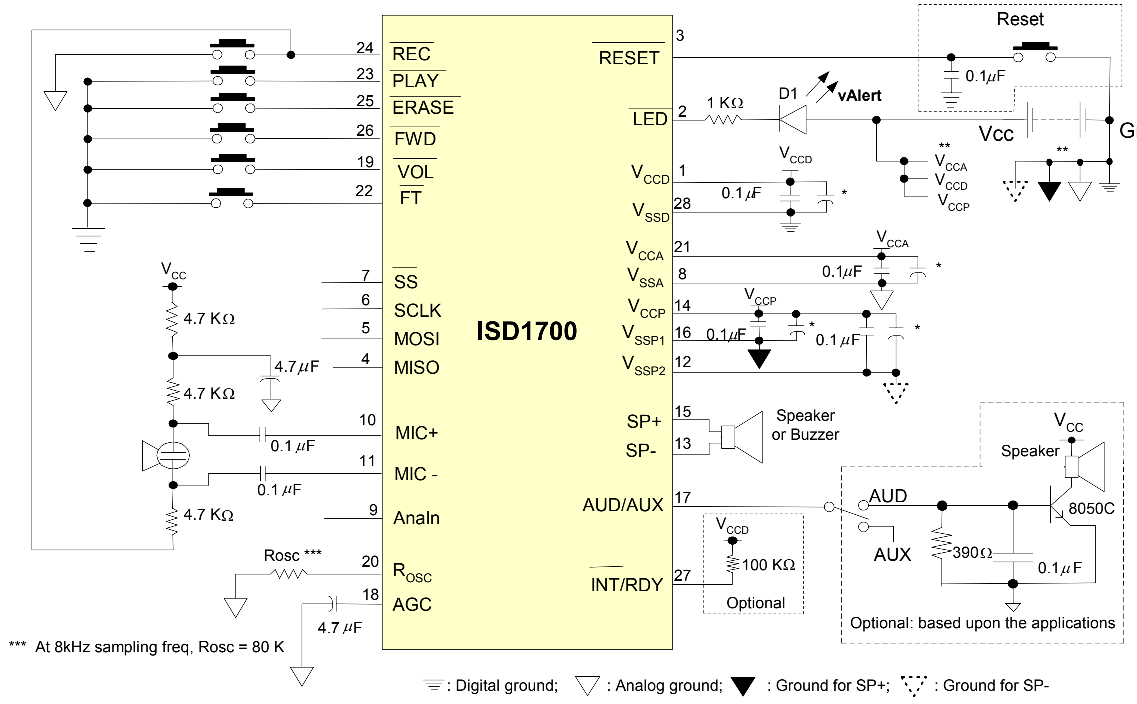
15 TYPICAL APPLICATION CIRCUITS

The following typical applications examples on ISD1700 Series are for references only. They make no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

The below notes apply to the following applications examples:

- * These capacitors may be needed in order to optimize for the best voice quality, which is also dependent upon the layout of the PCB. Depending on system requirements, they can be 10 µF, 4.7 µF or other values. Please refer to the applications notes or consult Winbond for layout advice.
- ** It is important to have a separate path for each ground and power back to the related terminals to minimize the noise. Also, the power supplies should be decoupled as close to the device as possible.

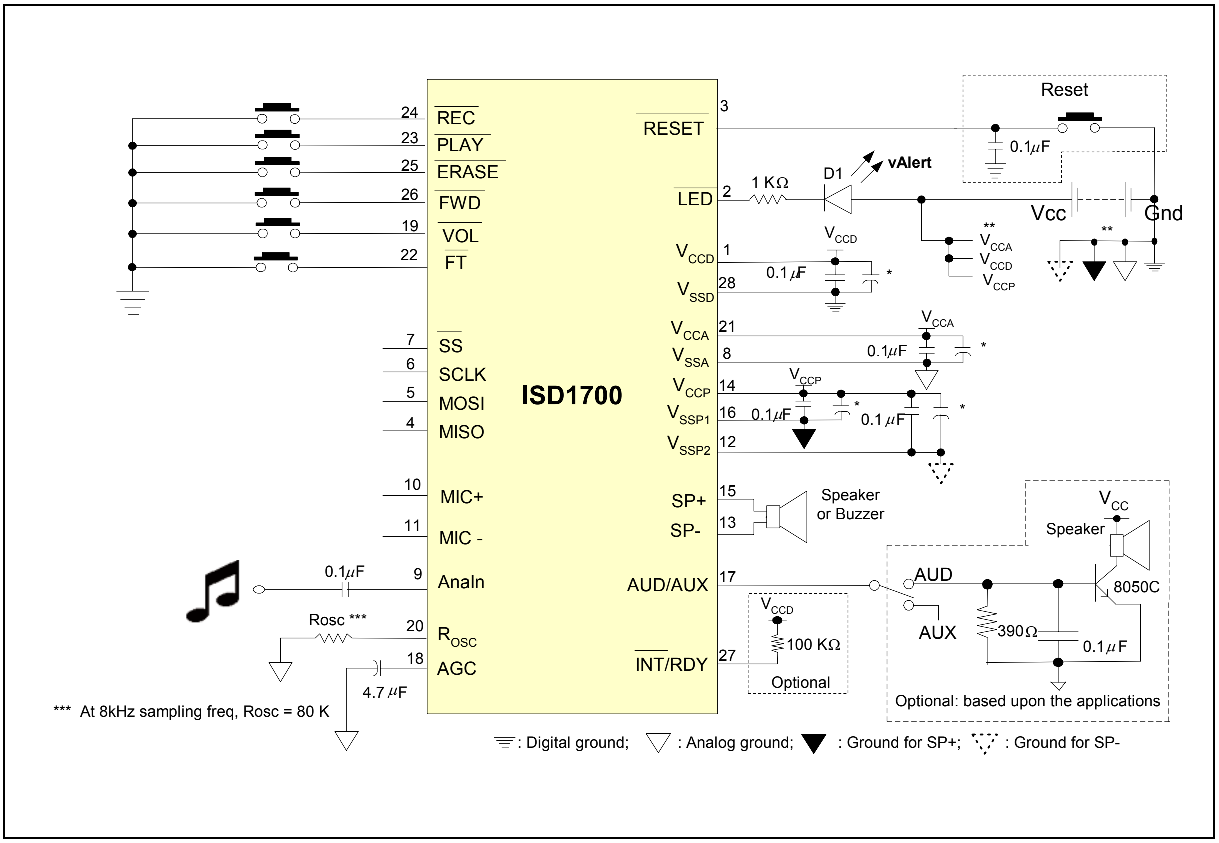
Example #1: Recording using microphone input via push-button controls



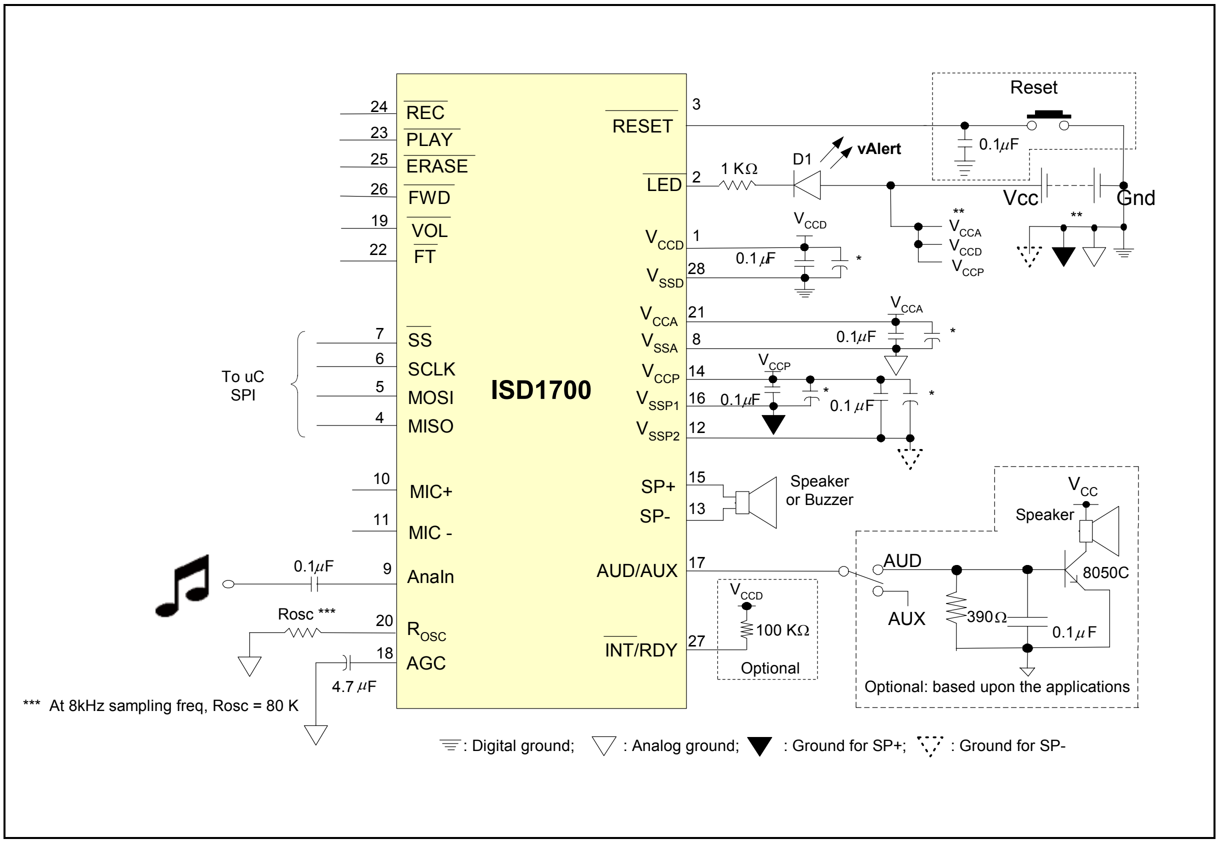
*** At 8kHz sampling freq, Rosc = 80 K

: Digital ground; ▽ : Analog ground; ▼ : Ground for SP+; ⛛ : Ground for SP-

Example #2: Recording using AnaIn input via push-button controls



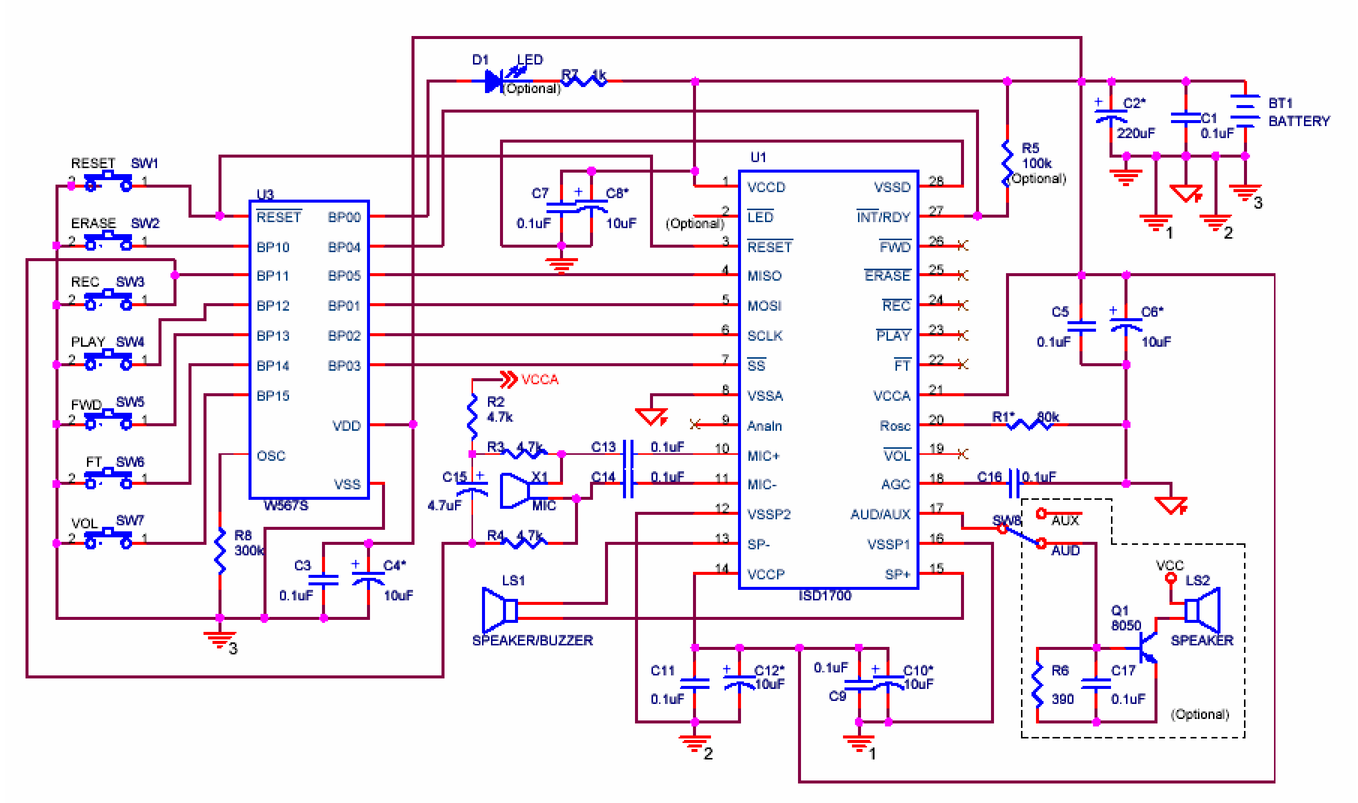
Example #3: Connecting the SPI Interface to a microcontroller



*** At 8kHz sampling freq, Rosc = 80 K

: Digital ground; ▽ : Analog ground; ▼ : Ground for SP+; ▽ : Ground for SP-

Example #4: Connecting the ISD1700 with PowerSpeech W567



15.1 GOOD AUDIO DESIGN PRACTICES

To ensure the highest quality of voice reproduction, it is important to follow good audio design practices in layout and power supply decoupling. See recommendations from below links or other Application Notes in our websites.

Design Considerations for ISD1700 Family

AN-CC1002 Design Considerations for ISD1700 Family

Good Audio Design Practices

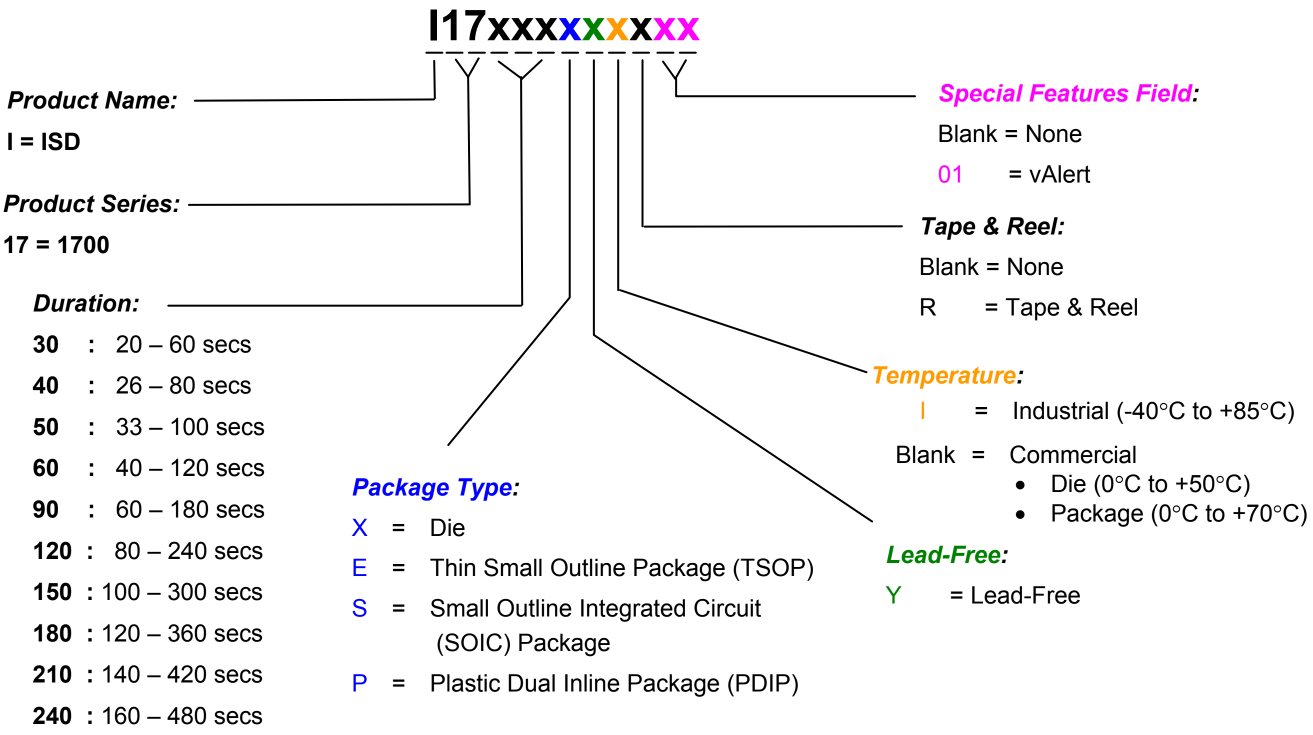
http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Layout Diagrams

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

16 ORDERING INFORMATION

Product Number Descriptor Key



I17xxxxxxxxx

Product Name:

I = ISD

Product Series:

17 = 1700

Duration:

30	:	20 – 60 secs
40	:	26 – 80 secs
50	:	33 – 100 secs
60	:	40 – 120 secs
90	:	60 – 180 secs
120	:	80 – 240 secs
150	:	100 – 300 secs
180	:	120 – 360 secs
210	:	140 – 420 secs
240	:	160 – 480 secs

Package Type:

X	=	Die
E	=	Thin Small Outline Package (TSOP)
S	=	Small Outline Integrated Circuit (SOIC) Package
P	=	Plastic Dual Inline Package (PDIP)

Special Features Field:

Blank = None

01 = vAlert

Tape & Reel:

Blank = None

R = Tape & Reel

Temperature:

I = Industrial (-40°C to +85°C)

Blank = Commercial

- Die (0°C to +50°C)
- Package (0°C to +70°C)

Lead-Free:

Y = Lead-Free

When ordering ISD1700 devices, please refer to the above ordering scheme. Contact the local Winbond Sales Representatives for any questions and the availability.

For the latest product information, please contact the Winbond Sales/Rep or access Winbond's worldwide web site at http://www.winbond-usa.com

17 VERSION HISTORY

VERSION	DATE	DESCRIPTION
0	October 2006	Initial version

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