Future Technology
Devices International Ltd.

VINCULUM

BINDING USB TECHNOLOGIES

Vinculum VNC1L

Embedded USB Host Controller I.C.

The Vinculum VNC1L is the first of FTDI's Vinculum family of Embedded USB host controller integrated circuit devices. Not only is it able to handle the USB Host Interface, and data transfer functions but owing to the inbuilt MCU and embedded Flash memory, Vinculum can encapsulate the USB device classes as well. When interfacing to mass storage devices such as USB Flash drives, Vinculum also transparently handles the FAT File structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Vinculum provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available.

The VNC1L is available in Pb-free (RoHS compliant) compact 48-Lead LQFP package.

http://www.vinculum.com

1. Features

1.1 Hardware Features

- Single chip embedded USB host / slave controller I.C. device
- Entire USB protocol handled on the chip
- 8 / 32 bit V-MCU Core
- Twin DMA controllers for hardware acceleration
- Integrated 12 MHz to 48 MHz clock multiplier
- Integrated power-on-reset circuit with optional RESET# input pin
- 64k byte embedded Flash ROM program memory
- 4k byte internal data SRAM
- Standard USB firmware library supplied by FTDI
- Program or update firmware via USB Flash disk or UART interface
- Firmware easily upgradable in the field
- PROG# firmware programming control pin
- Two independent USB 2.0 Low speed / Full speed USB Host / Slave ports with integrated pull-up and pull-down resistors
- Four fully configurable data I/O and control Buses
- UART interface mode for data I/O, firmware programming, and command monitor interface
- FIFO interface mode with 8 bit bi-directional data bus and simple 4 wire handshake for data I/O and command monitor interface
- SPI slave interface mode for data I/O and command monitor interface
- Up to 28 GPIO interface pins for data I/O and command monitor interface
- Interface to MCU / PLD / FPGA via UART, FIFO, or SPI interface
- Legacy PS/2 keyboard and mouse interfaces
- Multi-processor configuration capable
- Support for USB suspend and resume
- Support for bus powered, self powered, and high-power bus powered USB device configurations
- 3.3V operation with 5V safe inputs
- Low operating and USB suspend current (25mA running / 2mA stnadby)
- Fully compliant with USB 2.0 specification - USB full speed (12 Mbps) and low speed (1.5 Mbps) USB host and slave device compatible
- 0°C to 70°C operating temperature range
- Full driver support for target / slave applications
- Available in compact Pb-free and green 48 Pin LQFP package (RoHS compliant)
- Full range of reference designs and evaluation kits available

1.2 Standard Firmware

- USB slave device and USB Flash disk interface with selectable UART / FIFO / SPI interface or USB slave device as the command monitor port (VDIF firmware)
- FTDI USB slave device and USB Flash disk interface with selectable UART / FIFO / SPI interface as the command monitor port (VDAP firmware)
- USB Flash disk to USB Flash disk with GPIO command monitor interface (VF2F firmware)

1.3 Typical Applications

- Add USB host capability to embedded products
- Interface USB Flash drive to MCU / PLD / FPGA
- USB Flash drive to USB Flash drive file transfer interface
- Digital camera to USB Flash drive or other USB slave device interface
- PDA to USB Flash driver or other USB slave device interface
- MP3 Player to USB Flash drive or other USB slave device interface
- USB MP3 Player to USB MP3 Player
- Mobile phone to USB Flash drive or other USB slave device interface
- GPS to mobile phone interface
- Instrumentation USB Flash drive or other USB slave device interfacing
- Datalogger USB Flash drive or other USB slave device interface
- Set Top Box - USB device interface

2. Block Diagram

2.1 Simplified Block Diagram

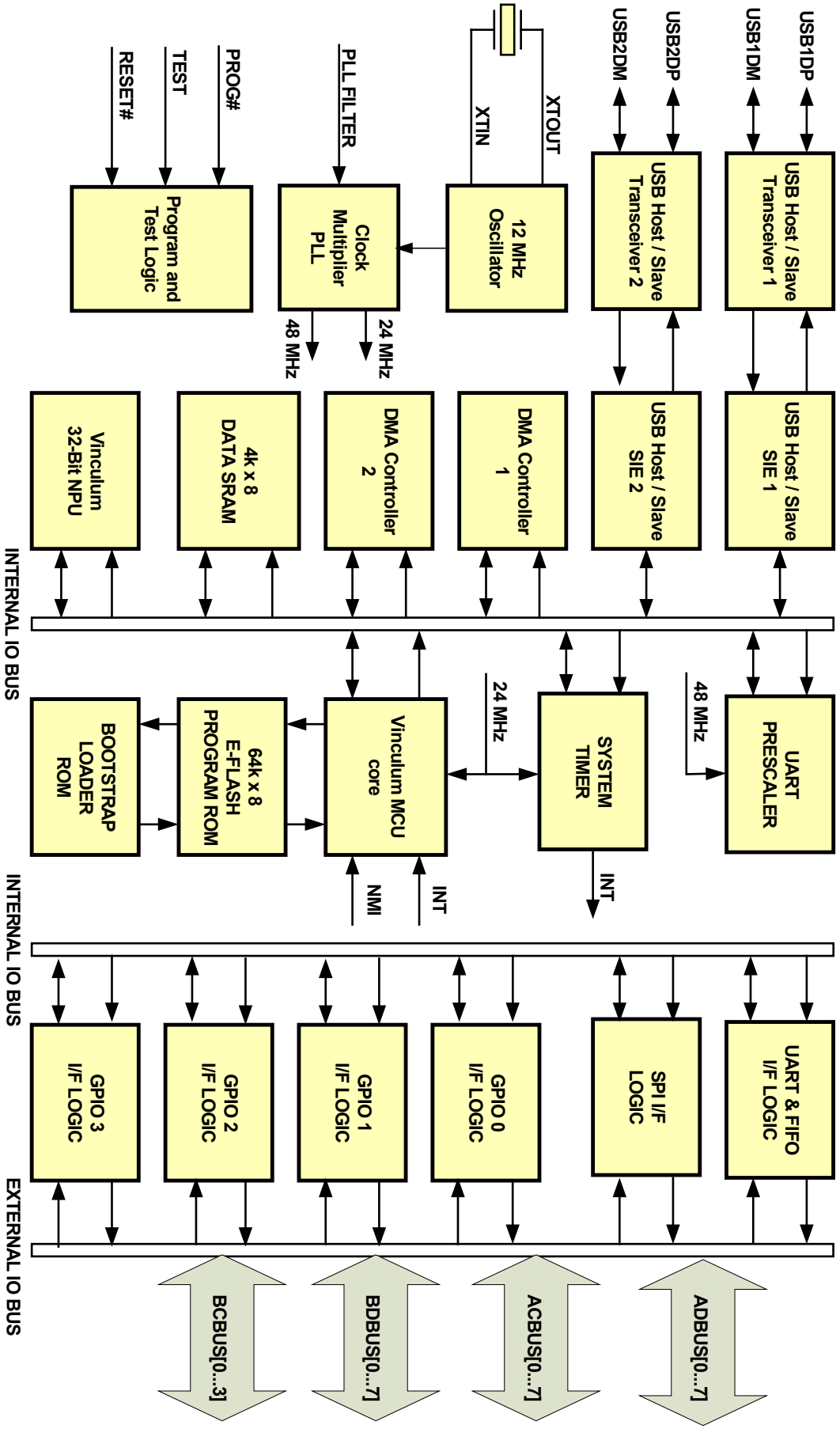


Figure 1 - Simplified Block Diagram

2.2 Functional Block Descriptions

USB Host / Slave Transceivers 1 and 2 - The two USB transceiver cells provide the USB host / slave physical USB 1.1 / USB 2.0 full-speed device interface. On each the output drivers provide 3.3V level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection. These cells also incorporate internal USB pull-up or pull down resistors as required for host or slave mode.

USB Host / Slave Serial Interface Engine (SIE) - These blocks handle the parallel to serial and serial to parallel conversion of the USB Physical layer including bit suffing / unstuffing, CRC generation / checking, USB frame generation and error checking.

12 MHz Oscillator - The 12MHz Oscillator cell generates a 12MHz reference clock input to the Clock Multiplier PLL from an exteral 12MHz crystal.

Clock Multiplier PLL - The Clock Multiplier PLL takes the 12MHz input from the Oscillator Cell and generates 24MHz and 48MHz reference clock signals, which is used by the USB SIE Blocks, the MCU core, System Timer and UART Prescaler blocks.

Program and Test Logic - this block provides a means of programming the onboard E-Flash memory. When PROG# is pulled low and the device is reset, the onboard E-Flash memory is bypassed by an internal hard coded BootStrap Loader ROM which contains code to allow the E-Flash memory to be programmed via commands to the UART interface. FTDI provides a software utility which allows the VNC1L to be programmed using this method. The TEST pin is used in manufacturing to enhance the testability of the various internal blocks and should be tied to GND.

DMA Controller 1 and 2 - The twin DMA controllers in the VNC1L greatly enhance performance by allowing data from the two USB SIE controllers, UART, FIFO and SPI to be transferred between each other via the data SRAM with minimal MCU intervention.

Data SRAM - This 4k x 8bit block acts as the data (variable) memory for the Vinculum MCU, though it can also be accessed transparently to the MCU by the twin DMA controllers.

NPU (Numeric CoProcessor) - Most Vinclum MCU operations are 8-bit, however there are some scenarios such as transversing disk FAT tables which involve extensive 32 bit arithmetic. In order to speed up these operations, the MCU has a dedicated 32 bit co-processor block.

UART Prescaler - this block provides the master transmit / receive clock for the UART block. By varying the prescalar value, the baud rate of the UART can be adjusted over a range of 300 baud to 1M baud.

SYSTEM TIMER - The system timer provides a regular interrupt to the Vinculum MCU, typically at 1mS intervals. This is used by the MCU to provide timeouts and other timing functions.

VINCULUM MCU CORE - The “heart” of the VNC1L is the VMCU core based on FTDI’s proprietary 8-bit embedded MCU (EMCU) architectiure. VMCU has a Harvard architecture i.e. separate code and data space and supports 64k byes of program code, 64k byes of (paged) data space and 256 bytes of IO space. It uses “enhanced CISC” technology - typically VNCU instructions would replace several lines of code in conventional CISC or RISC processors giving RISC like performance in a CISC architecture with the advantage over both of excellent code compression in the program ROM space.

E-FLASH Program ROM - The VNCL1L has 64k bytes of embedded Flash (E-Flash) memory. No special programming voltages are necessary for programming the onboard E-FLASH as these are provided internally on-chip. Common methods of programming the E-FLASH (both under control of the VMCU) are via the UART by pulling the PROG# pin low and resetting the device OR by using the programming via a USB FLASH drive feature provided in many of the VNC1L firmware packages.

BOOTSTRAP LOADER ROM - This is a small block of hard encoded ROM (512 x 8 bits) whivh bypasses the main e_FLASH memory when PROG# is pulled low. This provides a means of programming the entire E-Flash memory via the UART interface.

UART and FIFO Logic - These provide optional serial and parallel interfaces to the VNC1L equivalent to the interfaces on FTDI’s FT232 and FT245 USB UART and FIFO products.

GPIO Blocks - general purpose IO pins. See the tables below to determine which are available for any specific configuration.

2. Device Pin Out and Signal Descriptions

2.1 48 Lead LQFP Pin Out

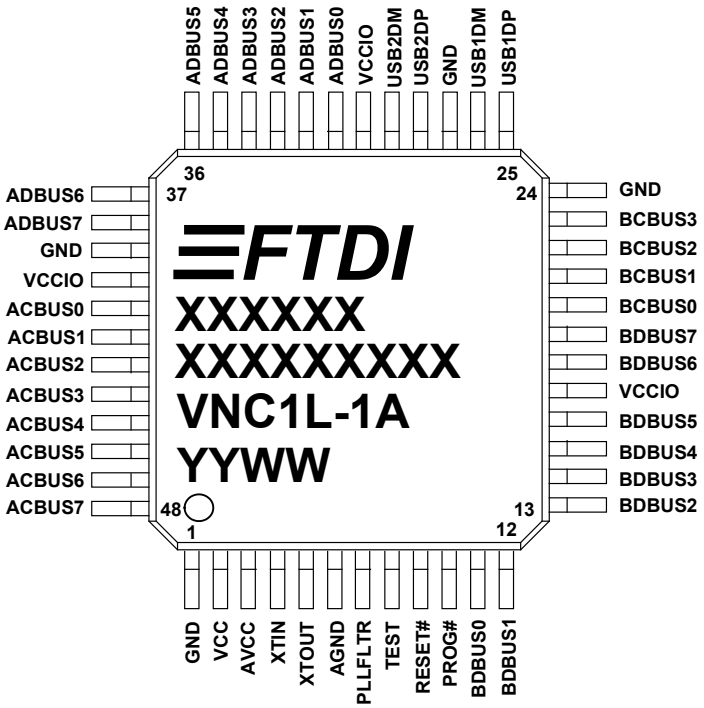


Figure 2 - 48 pin LQFP Package Pin Out

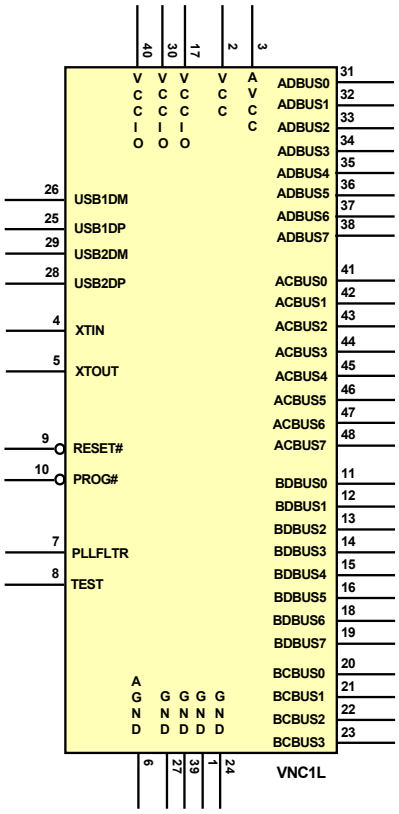


Figure 3 - VNC1L Pin Out - Schematic

2.2 48 Lead LQFP Package Signal Descriptions

Table 1 - Pin Out Description

Pin No.	Name	Type	Description				
USB Interface Group							
25	USB1DP	I/O	USB host / slave port 1 - USB Data Signal Plus with integrated pull up / pull down resistor.				
26	USB1DM	I/O	USB host / slave port 1 - USB Data Signal Minus with integrated pull up / pull down resistor.				
28	USB2DP	I/O	USB host / slave port 2 - USB Data Signal Plus with integrated pull up / pull down resistor.				
29	USB2DM	I/O	USB host / slave port 2 - USB Data Signal Minus with integrated pull up / pull down resistor.				
Power and Ground Group							
1, 24, 27, 39	GND	PWR	Device ground supply pins				
2	VCC	PWR	3.3V supply to the device core.				
3	AVCC	PWR	+3.3V supply to the internal clock multiplier. This pin requires a 100 nF decoupling capacitor.				
6	AGND	PWR	Device analog ground supply for internal clock multiplier				
17, 30, 40	VCCIO	PWR	+3.3V supply to the ADBUS, ACBUS, BDBUS and BCBUS Interface pins (11...16, 18...23, 31...38, 41...48).				
Miscellaneous Signal Group							
4	XTIN	Input	Input to 12MHz Oscillator Cell. Connect 12 MHz crystal across pins 4 and 5, with suitable loading capacitors to GND. This pin can also be driven by an external 12 MHz clock signal. Note that the switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level, or a.c. coupled to centre around VCC/2.				
5	XTOUT	Output	Output from 12MHz Oscillator Cell. Connect 12 MHz crystal across pins 4 and 5, with suitable loading capacitors to GND. XTOUT stops oscillating during USB suspend, so take care using this signal to clock external logic.				
7	PLLFLTR	Input	External PLL filter circuit input. RC filter circuit must be fitted on this pin.				
8	TEST	Input	Puts the device into I.C. test mode. Must be tied to GND for normal operation.				
9	RESET#	Input	Can be used by an external device to reset the VNC1L. This pin can be used in combination with PROG# and the UART interface to program firmware into the VNC1L. If not required pull up to VCC via a 10 kΩ resistor.*				
10	PROG#	Input	This pin is used in combination with the RESET# pin and the UART interface to program firmware into the VNC1L.*				
Data and Control Bus Signals							
				Interface Mode			
				UART Interface	Parallel FIFO Interface	SPI Slave Interface	I/O Port
11	BDBUS0	I/O	5V safe bidirectional data / control bus, BD bit 0				PortBD0
12	BDBUS1	I/O	5V safe bidirectional data / control bus, BD bit 1				PortBD1
13	BDBUS2	I/O	5V safe bidirectional data / control bus, BD bit 2				PortBD2
14	BDBUS3	I/O	5V safe bidirectional data / control bus, BD bit 3				PortBD3
15	BDBUS4	I/O	5V safe bidirectional data / control bus, BD bit 4				PortBD4
16	BDBUS5	I/O	5V safe bidirectional data / control bus, BD bit 5				PortBD5
18	BDBUS6	I/O	5V safe bidirectional data / control bus, BD bit 6				PortBD6
19	BDBUS7	I/O	5V safe bidirectional data / control bus, BD bit 7				PortBD7
20	BCBUS0	I/O	5V safe bidirectional data / control bus, BC bit 0	PS2Clk1**	PS2Clk1**	PS2Clk1**	PortBC0
21	BCBUS1	I/O	5V safe bidirectional data / control bus, BC bit 1	PS2Data1**	PS2Data1**	PS2Data1**	PortBC1
22	BCBUS2	I/O	5V safe bidirectional data / control bus, BC bit 2	PS2Clk2**	PS2Clk2**	PS2Clk2**	PortBC2
23	BCBUS3	I/O	5V safe bidirectional data / control bus, BC bit 3	PS2Data2**	PS2Data2**	PS2Data2**	PortBC3
31	ADBUS0	I/O	5V safe bidirectional data / control bus, AD bit 0	TXD	D0	SCLK	PortAD0
32	ADBUS1	I/O	5V safe bidirectional data / control bus, AD bit 1	RXD	D1	SDI	PortAD1
33	ADBUS2	I/O	5V safe bidirectional data / control bus, AD bit 2	RTS#	D2	SDO	PortAD2
34	ADBUS3	I/O	5V safe bidirectional data / control bus, AD bit 3	CTS#	D3	CS	PortAD3
35	ADBUS4	I/O	5V safe bidirectional data / control bus, AD bit 4	DTR#	D4		PortAD4
36	ADBUS5	I/O	5V safe bidirectional data / control bus, AD bit 5	DSR#	D5		PortAD5
37	ADBUS6	I/O	5V safe bidirectional data / control bus, AD bit 6	DCD#	D6		PortAD6
38	ADBUS7	I/O	5V safe bidirectional data / control bus, AD bit 7	RI#	D7		PortAD7
41	ACBUS0	I/O	5V safe bidirectional data / control bus, AC bit 0	TXDEN#	RXF#		PortAC0

Table 1 continued - Pin Out Description

42	ACBUS1	I/O	5V safe bidirectional data / control bus, AC bit 1		TXE#		PortAC1
43	ACBUS2	I/O	5V safe bidirectional data / control bus, AC bit 2		WR		PortAC2
44	ACBUS3	I/O	5V safe bidirectional data / control bus, AC bit 3		RD#		PortAC3
45	ACBUS4	I/O	5V safe bidirectional data / control bus, AC bit 4				PortAC4
46	ACBUS5	I/O	5V safe bidirectional data / control bus, AC bit 5				PortAC5
47	ACBUS6	I/O	5V safe bidirectional data / control bus, AC bit 6				PortAC6
48	ACBUS7	I/O	5V safe bidirectional data / control bus, AC bit 7. To use a 12 MHz crystal with the VNC1L fit a 47 kΩ pull-down resistor. Alternatively, fitting a 47 kΩ pull-up resistor on this pin will switch off the internal clock multiplier, allowing the device to be fed with an external 48Mz clock signal into XTIN.				PortAC7

* These pins are pulled to VCC via internal 200kΩ resistors.
** PS/2 Ports can be available while UART, FIFO, or SPI interface is enabled.

2.3 UART Interface Signal Descriptions

Table 4 - Data and Control Bus Signal Mode Options - UART Interface

Pin No.	Name	Type	Description
31	TXD	Output	Transmit asynchronous data output
32	RXD	Input	Receive asynchronous data input
33	RTS#	Output	Request To Send Control Output / Handshake signal
34	CTS#	Input	Clear To Send Control Input / Handshake signal
35	DTR#	Output	Data Terminal Ready Control Output / Handshake signal
36	DSR#	Input	Data Set Ready Control Input / Handshake signal
37	DCD#	Input	Data Carrier Detect Control Input
38	RI#	Input	Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend.
41	TXDEN	Output	Enable Transmit Data for RS485 designs

2.4 Parallel FIFO Interface Signal Descriptions and Timing Diagrams

Table 5 - Data and Control Bus Signal Mode Options - Parallel FIFO Interface

Pin No.	Name	Type	Description
31	D0	I/O	FIFO Data Bus Bit 0
32	D1	I/O	FIFO Data Bus Bit 1
33	D2	I/O	FIFO Data Bus Bit 2
34	D3	I/O	FIFO Data Bus Bit 3
35	D4	I/O	FIFO Data Bus Bit 4
36	D5	I/O	FIFO Data Bus Bit 5
37	D6	I/O	FIFO Data Bus Bit 6
38	D7	I/O	FIFO Data Bus Bit 7
41	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again.
42	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low.
43	WR	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low.
44	RD#	INPUT	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low.

Figure 4 - FIFO Read Cycle

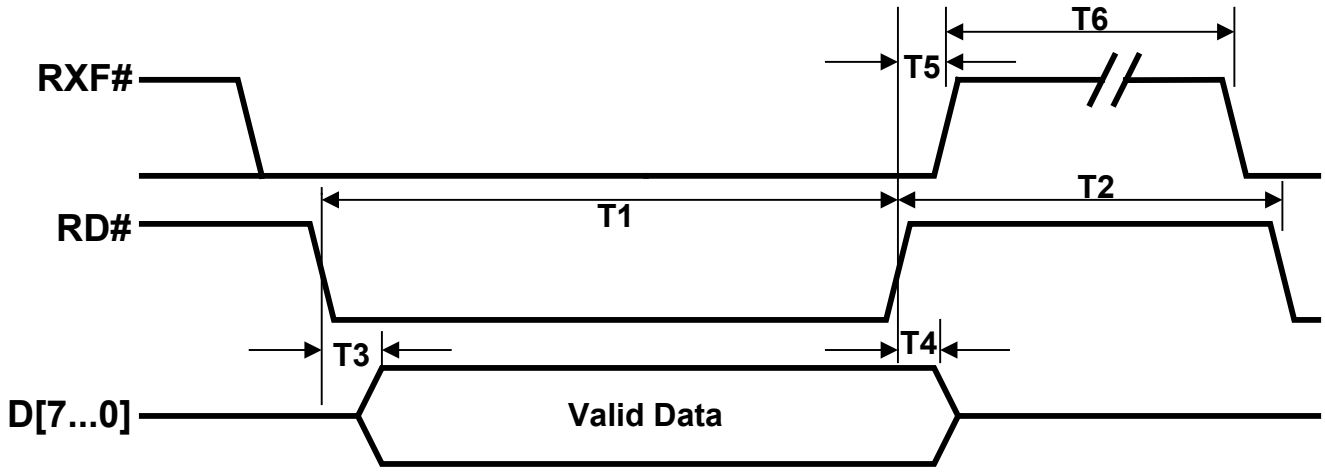


Table 6 - FIFO Read Cycle Timings

Time	Description	Min	Max	Unit
T1	RD Active Pulse Width	50	-	ns
T2	RD to RD Pre-Charge Time	50 + T6	-	ns
T3	RD Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD Inactive*	0	-	ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF Inactive After RD Cycle	80	-	ns

* Load = 30pF

Figure 5 - FIFO Write Cycle

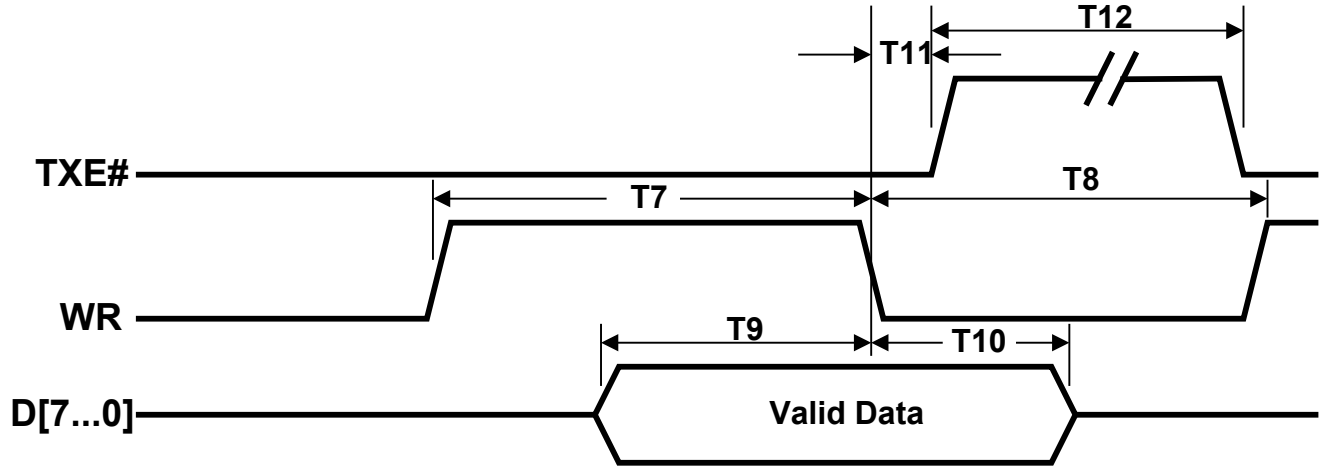


Table 7 - FIFO Write Cycle Timings

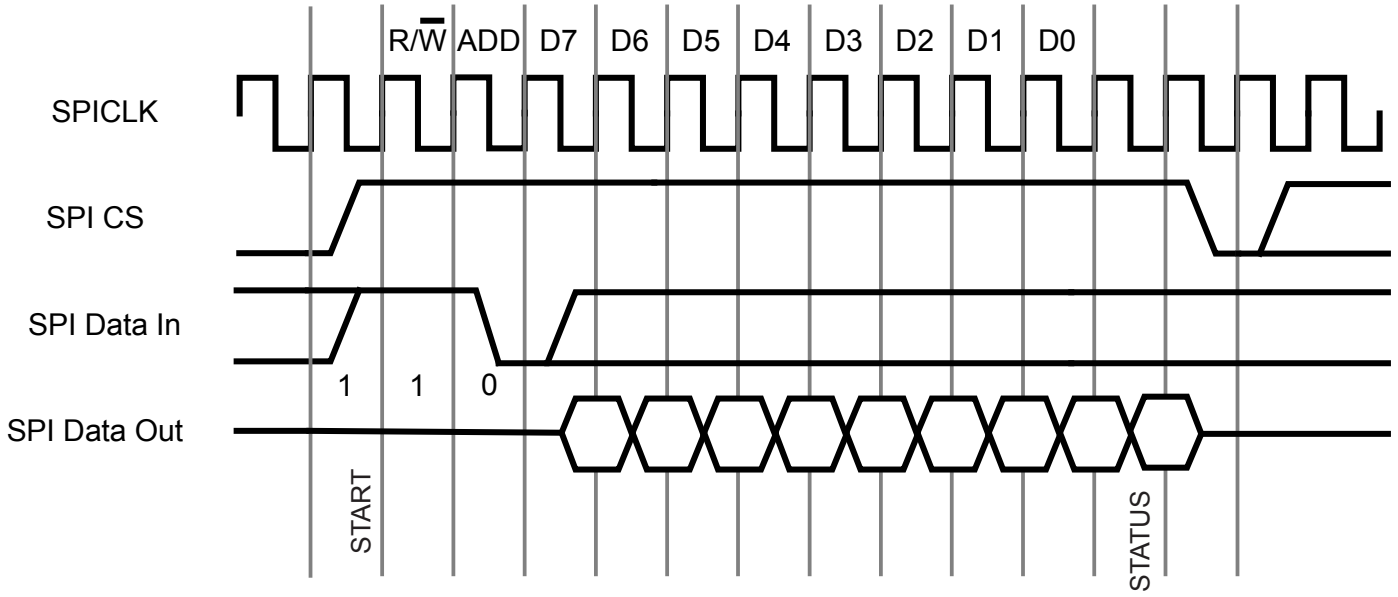
Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50	-	ns
T8	WR to RD Pre-Charge Time	50	-	ns
T9	Data Setup Time before WR Inactive	20	-	ns
T10	Data Hold Time from WR Inactive	0	-	ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE Inactive After WR Cycle	80	-	ns

2.5 SPI Interface Signal Descriptions and Timing Diagrams

Table 8 - Data and Control Bus Signal Mode Options - SPI Interface

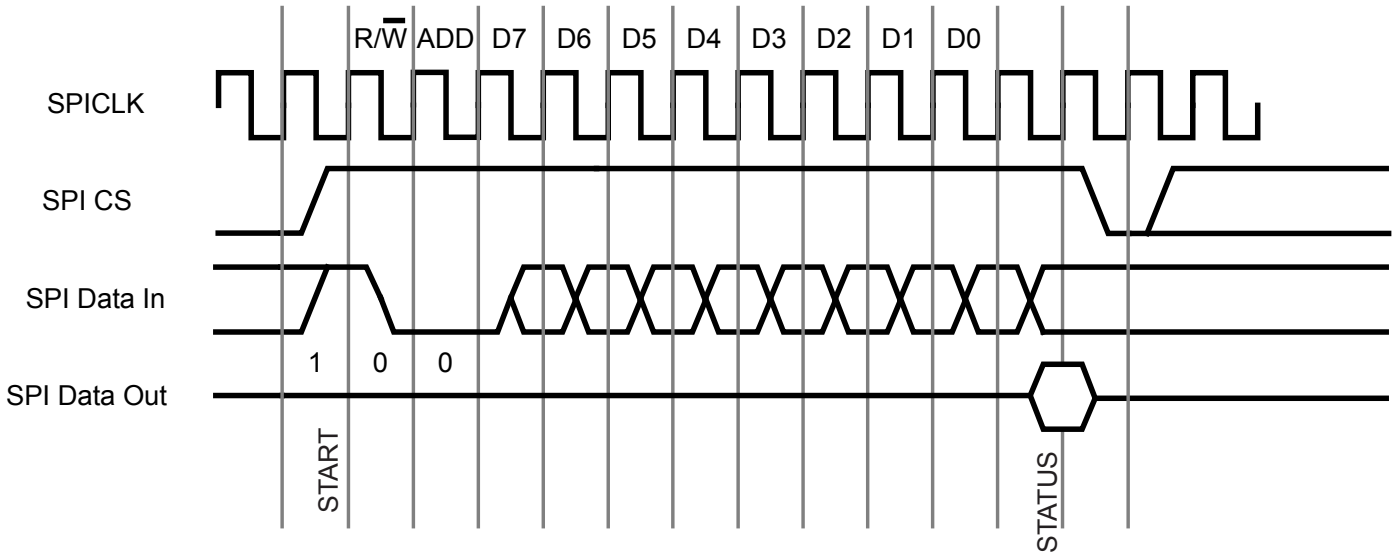
Pin No.	Name	Type	Description
31	SCLK	Input	SPI Clock input, 12MHz maximum.
32	SDI	Input	SPI Serial Data Input
33	SDO	Output	SPI Serial Data Output
34	CS	Input	SPI Chip Select Input

Figure 6 - SPI Slave Data Read Cycle



From Start - SPI CS must be held high for the entire read cycle, and must be taken low for at least one clock period after the read is completed. The first bit on SPI Data In is the R/W bit - inputting a '1' here allows data to be read from the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is read from. During the SPI read cycle a byte of data will start being output on SPI Data Out on the next clock cycle after the address bit, MSB first. After the data has been clocked out of the chip, the status of SPI Data Out should be checked to see if the data read is new data. A '0' level here on SPI Data Out means that the data read is new data. A '1' indicates that the data read is old data, and the read cycle should be repeated to get new data. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 7 - SPI Slave Data Write Cycle



From Start - SPI CS must be held high for the entire write cycle, and must be taken low for at least one clock period after the write is completed. The first bit on SPI Data In is the R/W bit - inputting a '0' here allows data to be written to the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status

register (‘1’) is written to. During the SPI write cycle a byte of data can be input to SPI Data In on the next clock cycle after the address bit, MSB first. After the data has been clocked in to the chip, the status of SPI Data Out should be checked to see if the data read was accepted. A ‘0’ level on SPI Data Out means that the data write was accepted. A ‘1’ indicates that the internal buffer is full, and the write should be repeated. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

Figure 8 - SPI Slave Data Timing Diagrams

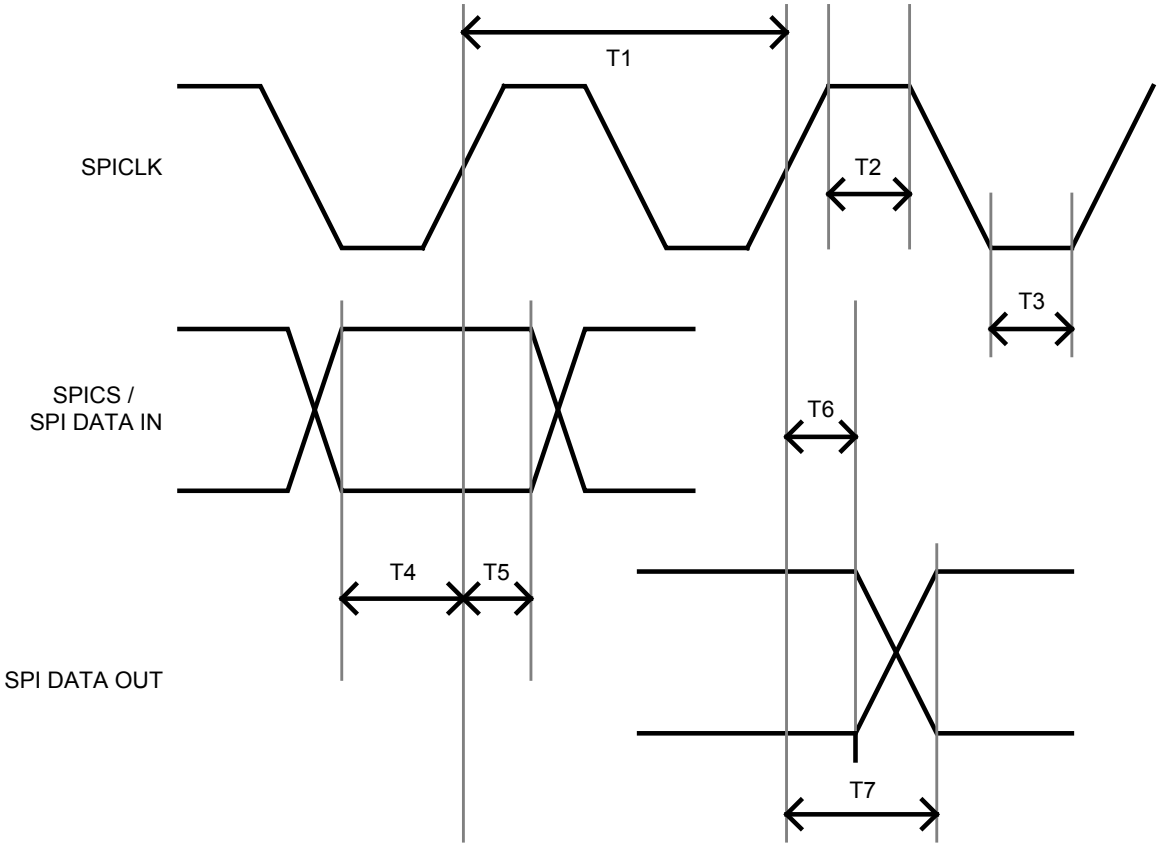


Table 9 - SPI Slave Data Timing

Time	Description	Min	Typical	Max	Unit
T1	SPICLK Period	83	-	-	ns
T2	SPICLK High	20	-	-	ns
T3	SPICLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Hold TIme	10	-	-	ns
T6	Output Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 10 - Status Register (ADD = ‘1’)

Bit	Description
0	RXF#
1	TXE#
2	-
3	-
4	RXF IRQEn
5	TXE IRQEn
6	-
7	-

2.6 PS/2 Keyboard and Mouse Interface

Table 11 - Data and Control Bus Signal Mode Options - PS/2 Keyboard and Mouse Interface

Pin No.	Name	Type	Description
20	PS2Clk1	I/O	PS/2 Keyboard or Mouse interface 1 clock signal
21	PS2Data1	I/O	PS/2 Keyboard or Mouse interface 1 data signal
22	PS2Clk2	I/O	PS/2 Keyboard or Mouse interface 2 clock signal
23	PS2Data2	I/O	PS/2 Keyboard or Mouse interface 2 data signal

3. Package Parameters

3.1 LQFP-48 Dimensions

The VNC1L is supplied in a 48 pin LQFP package as standard.

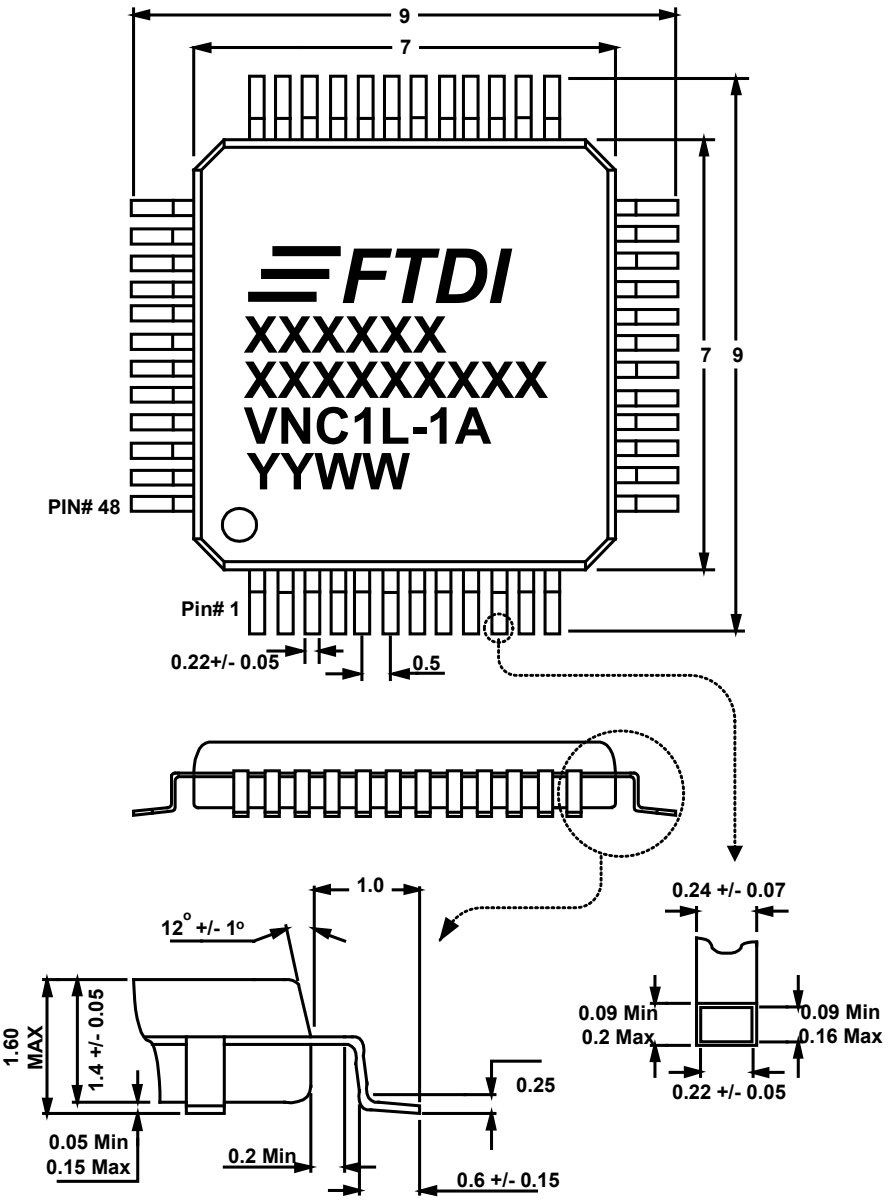


Figure 9 - LQFP-48 Package Dimensions

The VNC1L is supplied in a RoHS compliant 48 pin LQFP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package has a 7.00mm x 7.00 mm body (9.00 mm x 9.00 mm including pins). The pins are on a 0.50 mm pitch. The above mechanical drawing shows the LQFP-48 package – all dimensions are in millimetres.

The date code format is **YYWW** where WW = 2 digit week number, YY = 2 digit year number.

An alternative 6mm x 6mm leadless QFN package is also available for projects where PCB area is critical. Contact FTDI for availabillity.

3.2 Solder Reflow Profile

The VNC1L is supplied in Pb free 48 LD LQFP package. The recommended solder reflow profile is shown in below.

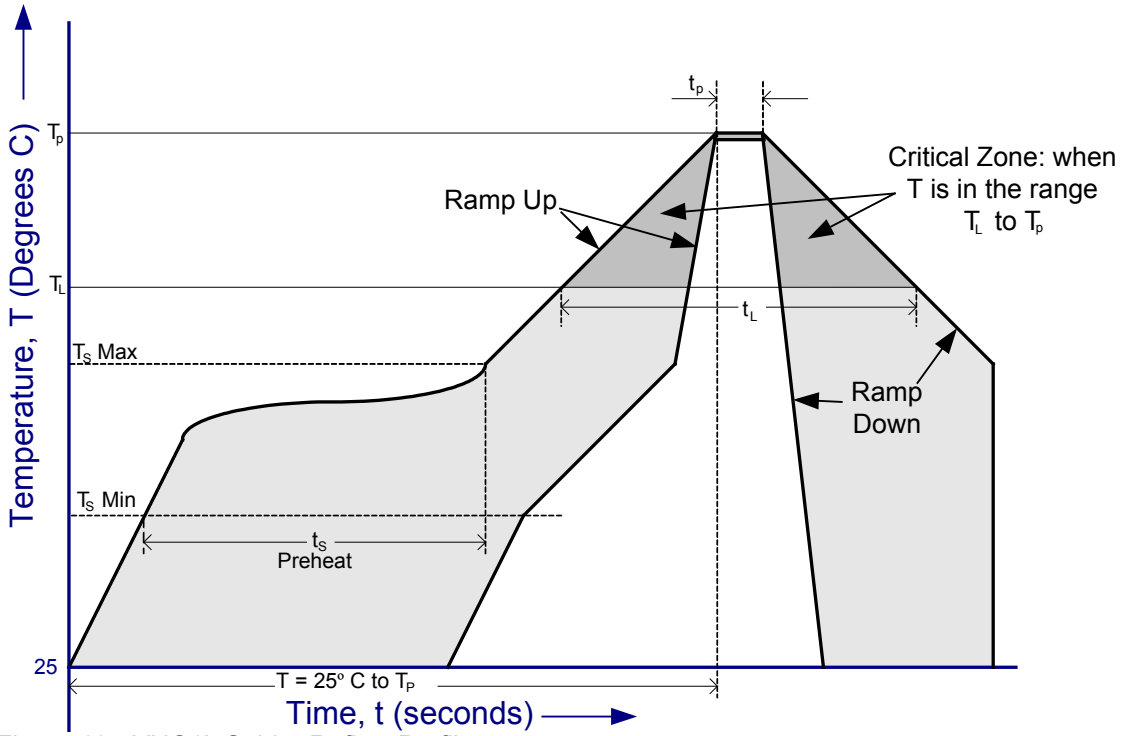


Figure 10 - VNC1L Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 4. Values are shown for both a completely Pb free solder process (i.e. the VNC1L is used with Pb free solder), and for a non-Pb free solder process (i.e. the VNC1L is used with non-Pb free solder).

Table 12 - Reflow Profile Parameter Values

Profile Feature	*Pb Free Solder Process*	*Non-Pb Free Solder Process*
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_S Min.) - Temperature Max (T_S Max.) - Time (t_S Min to t_S Max)	 150°C 200°C 60 to 180 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_P)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_P)	20 to 40 seconds	10 to 30 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

4. Device Characteristics and Ratings

4.1 Absolute Maximum Ratings

The absolute maximum ratings for the VNC1L devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Table 13 - Absolute Maximum Ratings

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	0°C to 70°C	Degrees C.
Vcc Supply Voltage	0 to 3.6	V
D.C. Input Voltage - USBDP and USBDM	--0.5 to +(Vcc +0.5)	V
D.C. Input Voltage - High Impedance Bidirectionals	-0.5 to +5.00	V
D.C. Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
D.C. Output Current - Outputs	8	mA
DC Output Current - Low Impedance Bidirectionals	8	mA
Power Dissipation (Vcc = 3.6V)	250	mW

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

4.2 DC Characteristics

DC Characteristics (Ambient Temperature = 0°C to +70°C)

Table 14 - Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	3.0	3.3	3.6	V	
Vcc2	VCCIO Operating Supply Voltage	3.0	3.3	3.6	V	
Icc1	Operating Supply Current	-	25	-	mA	Normal Operation
Icc2	Operating Supply Current	1	-	2	mA	USB Suspend

Table 15 - UART and CBUS I/O Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	Vcc-0.4			V	I source = 8mA
Vol	Output Voltage Low			0.4	V	I sink = 8mA
Vin	Input Switching Threshold	0.8	1.4	2.0	V	**

Table 16 - RESET# and PROG# Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Vin	Input Switching Threshold	0.8	1.4	2.0	V	

Table 17 - USB I/O Pin (USBDP, USBDM) Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	
UVol	I/O Pins Static Output (Low)	0		0.3	V	
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	28		44	Ohms	***

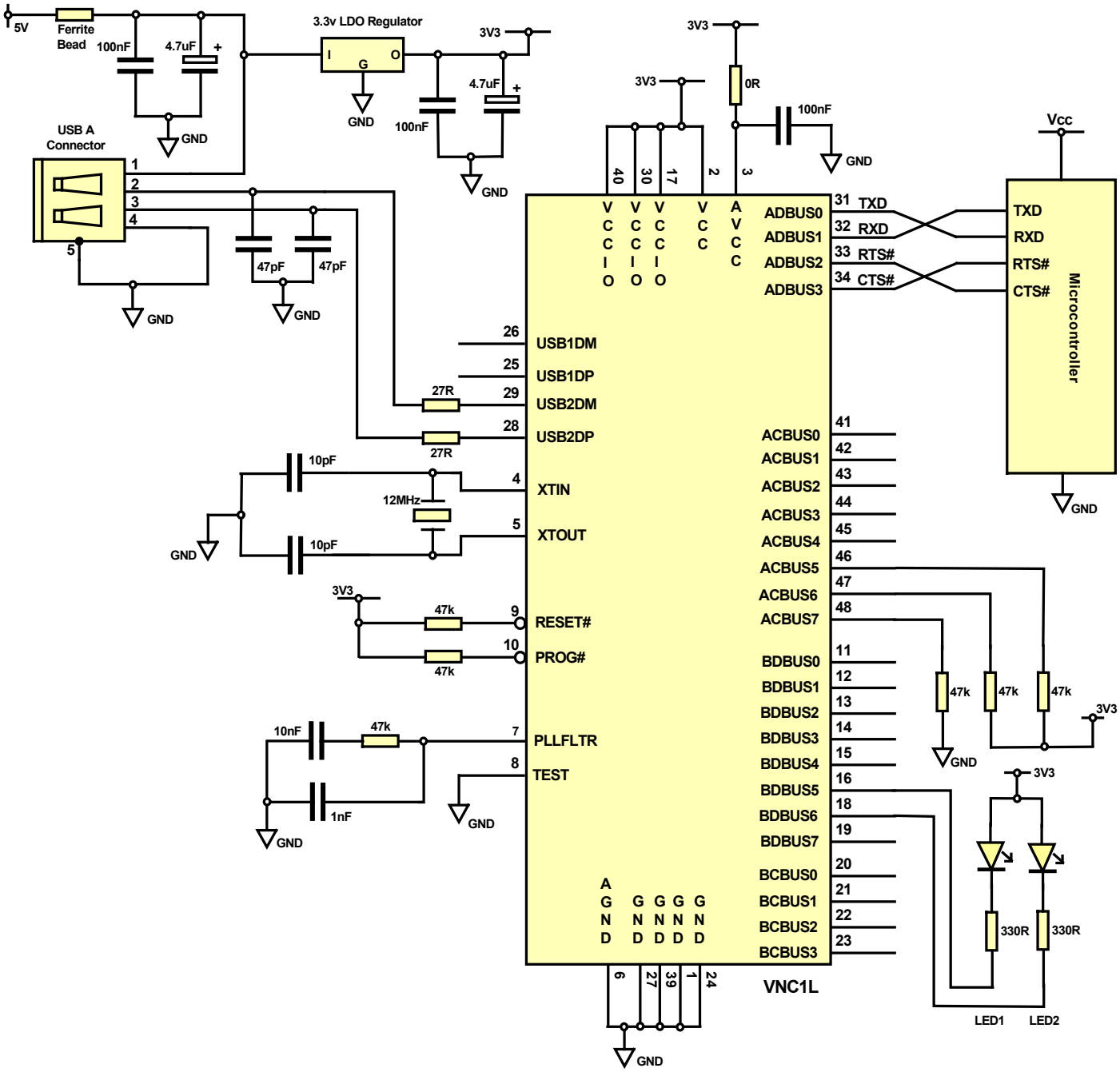
***Driver Output Impedance includes the external USB series resistors on USBDP and USBDM pins.

Table 18 - XTIN, XTOUT Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High		0.6		V	Fosc = 12MHz
Vol	Output Voltage Low		0.2		V	Fosc = 12MHz
Vin	Input Switching Threshold		0.4		V	

5. Device Configurations

5.1 Example VNC1L Schematic (MCU - UART interface)



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