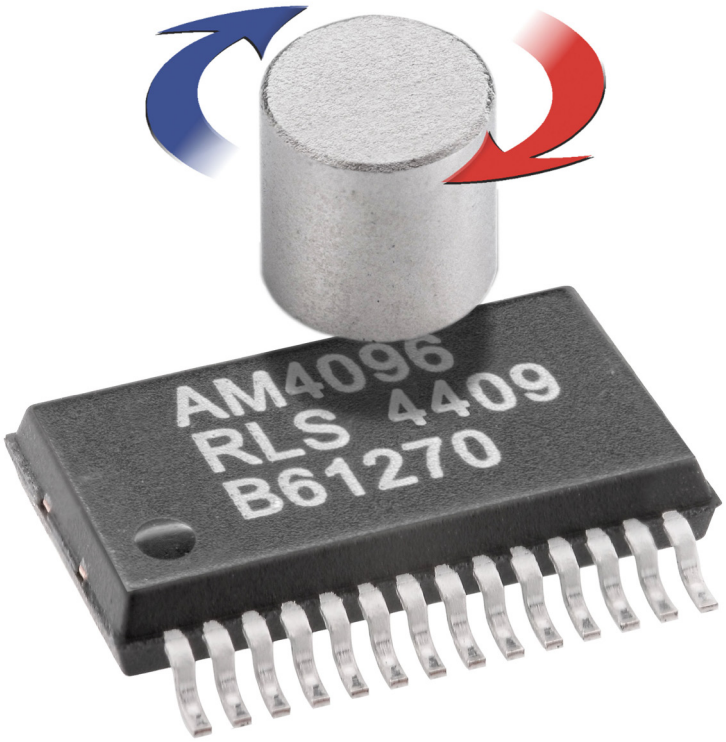
Data sheet
AM4096D02_06
Issue 6, 18th May 2018

AM4096 – 12 bit angular magnetic encoder IC



The AM4096 uses Hall sensor technology for sensing the magnetic field.

A circular array of sensors detects the perpendicular component of the magnetic field. The signals are summed then amplified. Sine and cosine signals are generated when the magnet rotates. The sine and cosine signals are factory calibrated for optimum performance.

From the sine and cosine values the angular position is calculated with a fast 12 bit interpolator. The calculated position is then output in various digital and analogue formats.

An inbuilt voltage regulator ensures stable conditions for the core of the chip and a more flexible power supply voltage. All inputs and outputs are related to the external supply voltage.

The AM4096 has many different setting options which are defined by the contents of internal registers. The zero position can be also set with an external pin. The settings of the chip are stored in an integrated EEPROM.

The registers and the EEPROM can be accessed through a serial two wire interface TWI.

With its compact size the AM4096 is especially suitable for different applications, including motor motion control and commutation, robotics, camera positioning, various encoder applications, battery powered devices and other demanding high resolution applications.

Output options:

- Incremental
- Serial SSI
- Serial two wire interface (TWI)
- UVW commutation output
- Linear voltage
- Tacho
- Analogue sinusoidal

- **Contactless angular position encoding over 360°**
- **12 bit absolute encoder**
- **Presetable zero position**
- **High speed operation to 60,000 rpm**
- **Power save mode for low current consumption**
- **5 V or 3 V power supply**
- **Integrated EEPROM**
- **SMD package SSOP28**
- **RoHS compliant (lead free)**

Block diagram

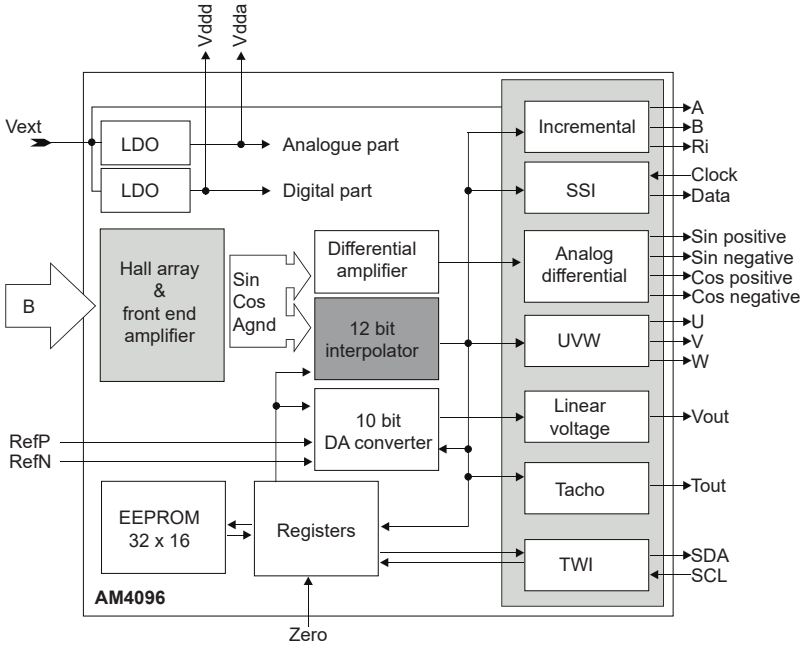


Fig. 1: AM4096 block diagram

Pin description

Some pins have more than one function. The function of those pins can be selected over the two wire serial interface and stored in the chip. All digital input pins all have a pull-down resistor except PSM pin.

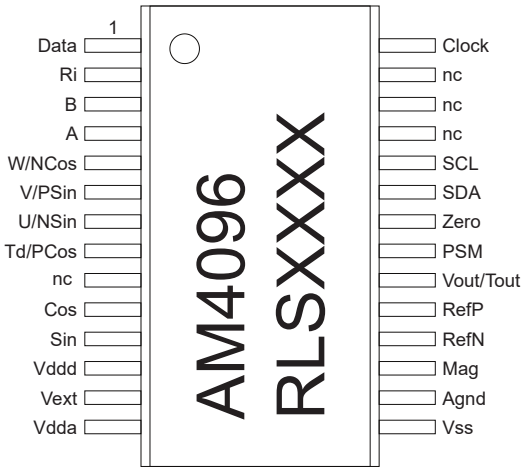


Fig. 2: Pin description for AM4096

Pin 1 (Data) is a digital output for serial SSI communication.

Pin 2 (Ri) is the quadrature incremental reference mark output.

Pin 3 (B) is the quadrature incremental output B.

Pin 4 (A) is the quadrature incremental output A.

Pin 5 (W/N_{Cos}) is the commutation digital output W or analogue differential buffered Cosine negative output.

Pin 6 (V/P_{Sin}) is the commutation digital output V or analogue differential buffered Sine positive output.

Pin 7 (U/N_{Sin}) is the commutation digital output U or analogue differential buffered Sine negative output.

Pin 8 (Td/P_{Cos}) is the tacho direction digital output or analogue differential buffered Cosine positive output.

Pin 9 is the test pin and must be left unconnected.

Pin 10 (Cos) is the single-ended cosine analogue output for filtering.

Pin 11 (Sin) is the single-ended sine analogue output for filtering.

Pin 12 (V_{ddd}) is the pin for filtering the power supply of the digital part of the chip. The power supply voltage is selectable between 3 V and 3.3 V.

Pin 13 (V_{ext}) is the external power supply pin (3 V to 5.5 V).

Pin 14 (V_{dda}) is the pin for filtering the power supply of the analogue part of the chip. The power supply voltage is selectable between 3 V and 3.3 V.

Pin 15 (V_{ss}) is the power supply pin 0 V.

Pin 16 (Agnd) is the pin for filtering analogue reference voltage (1.55 V).

Pin 17 (Mag) is the digital output for monitoring the magnet presence. If the output is high than the magnet distance is OK. If the distance is too small or too large, then the output voltage is low.

Pin 18 (R_{efN}) is the reference voltage input for defining the minimum output value of the linear voltage output.

Pin 19 (R_{efP}) is the reference voltage input for defining the maximum output value of the linear voltage output.

Pin 20 (V_{out}/T_{out}) is the linear voltage output or tacho output.

Pin 21 (PSM) is the digital input pin for power save mode operation. The input is floating and it must have defined input. When the input is low, the power save mode is inactive.

Pin 22 (Zero) is the digital input for zeroing the output position with internal 10k pull-down resistor. The zeroing is done at transition from low to high.

Pin 23 (SDA) is the data line for the two wire serial interface (TWI).

Pin 24 (SCL) is the clock line for the two wire serial interface (TWI).

Pins 25, 26 and 27 are test pins and must be left unconnected.

Pin 28 (Clock) is the digital clock input for SSI communication with internal 10k pull-down resistor.

Pin	Name	Pin description
1	Data	SSI data output
2	Ri	Incremental output Ri
3	B	Incremental output B
4	A	Incremental output A
5	W/N_{Cos}	Commutation output W/Cosine negative output
6	V/P_{Sin}	Commutation output V/Sine positive output
7	U/N_{Sin}	Commutation output U/Sine negative output
8	Td/P_{Cos}	Tacho direction output/Cosine positive output
9	NC	Factory test
10	Cos	Cosine analogue output for filtering
11	Sin	Sine analogue output for filtering
12	V_{ddd}	Digital power supply 3.0 / 3.3 V
13	V_{ext}	Power supply input 5 V
14	V_{dda}	Analogue power supply 3.0 / 3.3 V
15	V_{ss}	Power supply 0 V
16	Agnd	Analogue reference voltage
17	Mag	Output, that indicates magnet presence
18	R_{efN}	Lower reference input for voltage output
19	R_{efP}	Upper reference input for voltage output
20	V_{out}/T_{out}	Linear voltage output/Tacho output
21	PSM	Power save mode input
22	Zero	Zeroing input
23	SDA	TWI serial interface data line
24	SCL	TWI serial interface clock line
25	NC	Factory test
26	NC	Factory test
27	NC	Factory test
28	Clock	SSI clock input

Absolute maximum ratings

T_A = 22 °C unless otherwise noted.

Parameter	Symbol	Min.	Max.	Unit	Note
Supply voltage	V_{ext}	–0.3	5.5	V	
Input pin voltage	V_{in}	–0.3	5.5	V	
Input current (latch-up immunity)	I_{scr}	–100	100	mA	
Electrostatic discharge	ESD		2	kV	*
Operating junction temperature	T_j	–40	140	°C	
Storage temperature range	T_{st}	–40	150	°C	
Moisture sensitivity level			3		

* Human Body Model

Operating range conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
General						
Temperature range	T_O	–40	125		°C	
Temperature range for EEPROM write	T_{OE}	–40	115		°C	
Supply voltage	V_{ext}	3	5	5.5	V	
Supply current	I_{dd}	*	26	30	mA	*
Power-up time	t_p		1.5	2	ms	
Interpolator delay	t_{di}		0.7		µs	
Sensors delay	t_{ds}		10		µs	
Filtering delay	t_{df}		20		µs	**
Oscillator						
Oscillator frequency	f_{osc}	8	10	12	MHz	
Oscillator frequency temperature drift	TC_{osc}		–0.006		% / K	
f_{osc} power supply dependence	VC_{osc}		3		% / V	***
Digital outputs						
Saturation voltage hi (V_{ext} – V_{out})	V_{shi}	137		490	mV	I_{load} = 2mA
Saturation voltage lo	V_{slo}	124		339	mV	I_{loa} = 2mA
Rise time	t_r	4		12	ns	C_{load} = 15+3pF
Fall time	t_f	3		9	ns	C_{load} = 15+3pF
Digital inputs						
Threshold voltage hi	Vt_{hi}	0.39	0.5	0.59	V_{ext}	
Threshold voltage lo	Vt_{lo}	0.30	0.38	0.45	V_{ext}	
Hysteresis	Vt_{hys}	0.08	0.12	0.15	V_{ext}	

* When in power-save mode the average supply current is significantly reduced.
** Typical time delay is calculated for filter capacitors 10 nF.
*** Due to internal supply regulator only 3 V or 3.3 V is possible.

AM4096 programming

The AM4096 can be programmed over the two-wire serial interface (TWI) which is compatible with I²C protocol with a 400 kbps bit rate speed.

The TWI protocol allows the to interconnect up to 128 individually addressable devices using only two bi-directional bus lines, one for clock (SCL) and one for data (SDA). The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. All devices connected to the bus have individual addresses, and mechanisms for resolving bus contention are inherent in the TWI protocol.

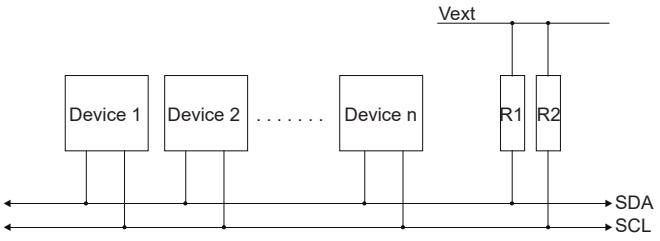


Fig. 3: TWI bus interconne

The TWI bus is a multi-master bus where one or more devices, capable of taking control of the bus, can be connected. Only Master devices can drive both the SCL and SDA lines while a Slave device is only allowed to issue data on the SDA line. Data transfer is always initiated by a Bus Master device. A high to low transition on the SDA line while SCL is high is defined to be a START condition (or a repeated start condition).

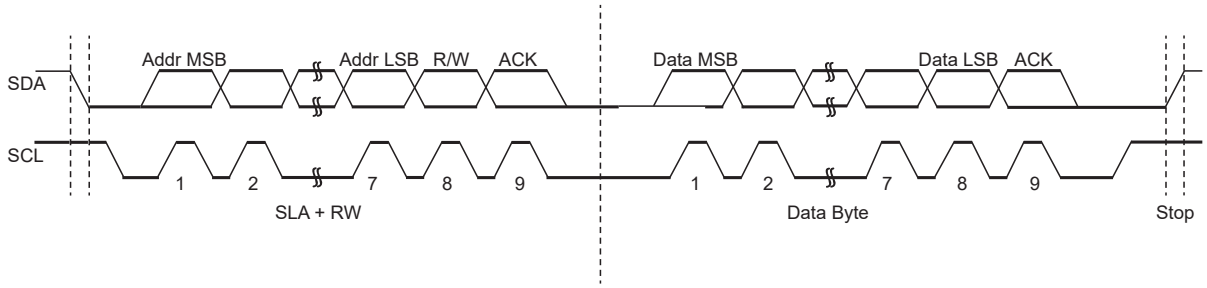


Fig. 4: TWI Address and Data Packet Format

A START condition is always followed by the (unique) 7 bit slave addresses and then by a Data Direction bit. The Slave device addressed now acknowledges to the Master by holding SDA low for one clock cycle. If the Master does not receive any acknowledge the transfer is terminated. Depending of the Data Direction bit, the Master or Slave now transmits 8 bit of data on the SDA line. The receiving device then acknowledges the data. Multiple bytes can be transferred in one direction before a repeated START or a STOP condition is issued by the Master. The transfer is terminated when the Master issues a STOP condition. A STOP condition is defined by a low to high transition on the SDA line while the SCL is high. If a Slave device cannot handle incoming data until it has performed some other function, it can hold SCL low to force the Master into a wait-state. All data packets transmitted on the TWI bus are 9 bits long, consisting of one data byte and an acknowledge bit. During a data transfer, the master generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An Acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

The AM4096 has a default slave address of 00h. This address can be changed for each device. The functionality of the device can be programmed on the addresses between 0 and 55 with 16 bit long words.

Address	Functionality
00–31	Read/Write EEPROM
32–35	Read registers for reading the output data
40–41	Write registers for factory tests
48–55	Read / Write registers with settings

The AM4096 device acts as a slave and supports two modes:

1. Master transmits to slave. This mode is used to write to the AM4096 address space. The 16 bit data word is divided into two 8 bit data frames. The ACK acknowledges are provided by the slave.

Fig. 5: Write data packet

After the EEPROM write packet (memory address 00 h – 1 Fh) the slave device can not be addressed for a time of 20 ms. In this time the slave is performing the internal EEPROM write process. If the device is addressed, no ACK is returned.

2. Combined format mode is used to read the AM4096 address space. If the EEPROM address space is addressed (00 h – 1 Fh), then the slave uses clock stretching during the internal EEPROM read time (minimum 20 µs).

Start	7 bit slave address	Write	ACK	8 bit mem. address	ACK	SR	7 bit slave address	Read	ACK	CLK stretching min. 20 µs	8 bit MSB data	ACK	8 bit LSB data	ACK	Stop

Fig. 6: EEPROM read data packet, with clock stretching

If the R or R/W registers are addressed, then the device response is immediate. After the two DATA packets the ACK is not verified.

Start	7 bit slave address	Write	ACK	8 bit mem. address	ACK	SR	7 bit slave address	Read	ACK	8 bit MSB data	ACK	8 bit LSB data	ACK	Stop

Fig. /: Register read data packet

Memory address space

		ADR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EEPROM	R/W	0	Pdint	AGCdis	-	Slowint	Pdtr		Pdie	Reg35	-	Addr						
		1	Abridis	Bufsel		Sign	Zin											
		2	Nfil								Daa	Hist						
		3	Dact	Dac		SSIcfg		-	-	Sth		UVW			Res			
	R	4	Factory settings data.															
		5																
		6	This part of EEPROM is locked.															
		7																
	R/W	8	Free EEPROM space															
		9																
		10																
		...																
		28																
		29																
	R	30	Device identification number. This part of EEPROM is locked.															
		31																
REGISTERS	R	32	SRCH	-	-	-	Rpos											
		33	SRCH	-	-	-	Apos											
		34		Weh	Wel	-												
		35	AGCgain				-	Thof	Tho									
		...	Not available															
	R/W	40	Only for testing. For normal operation must be zeros.															
		41																
		...	Not available															
	R/W	48	Pdint	AGCdis	-	Slowint	Pdtr		Pdie	Reg35	-	Addr						
		49	Abridis	Bufsel		Sign	Zin											
		50	Nfil								Daa	Hist						
		51	Dact	Dac		SSIcfg		-	-	Sth		UVW			Res			
	R	52	Factory settings data.															
		53																
		54	Those registers are locked.															
		55																

AM4096 has EEPROM and registers with 16 bit word organization. AM4096 operates according to the contents in registers. When the chip is powered-on the EEPROM content from address 0 to 7 is copied to the registers from 48 to 55. This is also done with every change in the EEPROM. Registers from 48 to 51 can be accessed for fast non-permanent setting changes. Registers from 32 to 35 can be used for fast readings of the measured data.

Description of parameters:

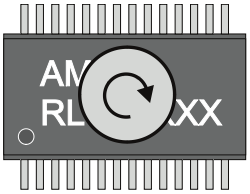
Parameter	Length	Description	Logic	Note
Pdint	1	Interpolator power	0 = on, 1 = off	Interpolator power can be switched off, if only analogue outputs are used.
AGCdis	1	AGC disable	0 = AGC on, 1 = AGC off	
Slowint	1	Interpolator delay	0 = on, 1 = off	It must always be set to 1. Currently it is not allowed to use value 0.
Pdtr	2	Internal power down rate	00 = 1:128, 01 = 1:256, 10 = 1:512, 11 = 1:1024	See power save mode description.
Pdie	1	Internal power down	0 = disabled, 1 = enabled	See power save mode description.
Reg35	1	Regulator voltage	0 = 3 V, 1 = 3.3 V	
Adr	7	Device address	From 0 to 127	Default address is set to 0.
Abridis	1	Enabling A B Ri outputs	0 = enabled, 1 = disabled	Incremental output can be disabled if not used.
Bufsel	1	Selects the output on pins U/ N_{Sin}, V/P_{Sin}, W/N_{Cos}, Td/P_{Cos}	0 = UVW, Tacho direction 1 =Sinusoidal differential	Interpolator may not work properly when sinusoidal differential analogue outputs are on.
Monsel	1	Test parameter		Must be zero.
Sign	1	Selects the output direction	0 = positive, 1 = negative	
Zin	12	Zero position data	0 = 0°, 4,095 = 360°	
Nfil	8	Test parameters		Must be zeros.
Daa	1	Output position selection	0 = relative, 1 = absolute	Absolute position is not affected by zeroing while relative position is.
Hist	7	Digital hysteresis value in LSB at 12 bit resolution	From 0 to 127	
Dact	1	Select the output on V_{out}/T_{out} pin	0 = position data on V_{out}/ T_{out} pin 1 = tacho data on V_{out}/T_{out} pin	
Dac	2	Linear voltage period selection	00 = 360°, 01 = 180°, 10 = 90°, 11 = 45°	
SSIcfg	2	SSI settings		See SSI description.
Sth	3	Tacho measuring range		See table in tacho output description.
UVW	3	UVW number of periods/turn	000 = 1, 001 = 2, 010 = 3, 011 = 4, ..., 111 = 8	
Res	3	Interpolation factor rate	000 = 4,096, 001 = 2,048, ... 110 = 64, 111 = 32	
SRCH	1	Output position data valid	0 = valid data 1 = data not valid yet	
Rpos	12	Relative position inf.	0 = 0°, 4,095 = 360°	
Apos	12	Absolute position inf.	0 = 0°, 4,095 = 360°	
Weh	1	Magnet too far status	0 = magnet distance ok, 1 = magnet is too far	
Wel	1	Magnet too close status	0 = magnet distance ok, 1 = magnet is too close	
Thof	1	Tacho overflow info	0 = speed in range, 1 = speed out of range	
Tho	10	Tacho output data	0 = 0, 1,023 = full measuring range	

3/5 V operation mode

The AM4096 can operate with power supply voltage from 3 V to 5.5 V. The outputs and inputs are supplied with the external voltage. The core of the chip is always powered with the regulated voltage from the LDO voltage regulator. The voltage of the regulator can be selected with the “Reg35” parameter between 3 V and 3.3 V. When the external power supply is from 3 V to 3.3 V the regulator voltage should be set to 3 V. When the external power supply voltage is from 3.3 V to 5.5 V the regulator voltage should be set to 3.3 V.

Outputs direction

The direction of the outputs can be changed by changing the “Sign” parameter. The arrow in picture shows clockwise (CW) rotation of the magnet. The picture is a top view of the magnet placed above the AM4096.



Sinusoidal analogue outputs for filtering

Agnd is an internally generated reference voltage. It is used as a zero level for the analogue signals, the voltage is typically 1.55 V. Pins 10 and 11 are unbuffered sinusoidal analogue outputs used for filtering and for testing purposes.

Unbuffered sinusoidal outputs:

Parameter	Symb.	Min	Typ	Max	Unit
Internal serial impedance	R_n		2		kΩ

The chart below shows the timing diagram for CW rotation of the recommended magnet.
Sinusoidal outputs produce one period of sine and cosine signal per turn with phase difference of 90°. Each signal has the same amplitude and minimum offset with respect to Agnd.
AGC controls the amplitude of the signals within 20%. AGC can be disabled if “AGCdis” parameter is set to 1.

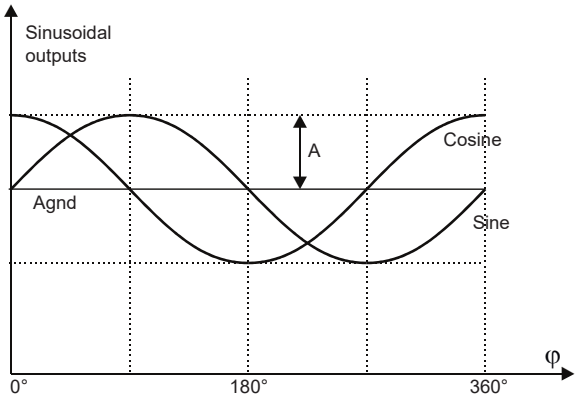


Fig. 8: Timing diagram for analogue output

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Amplitude	A	0.5	0.83	1.1	V	*
Vref voltage	V_{Vref}		1.55		V	
Max. frequency	f_{Max}		1000		Hz	

* Amplitude = 1/2 of peak to peak value.

Sinusoidal differential analogue outputs

Sinusoidal signals can be output as sinusoidal differential signals when the “BufSel” parameter is set to 1. The interpolator may not work properly when the differential analogue outputs are on. If analogue outputs are not needed then the “BufSel” parameter should be set to 0.

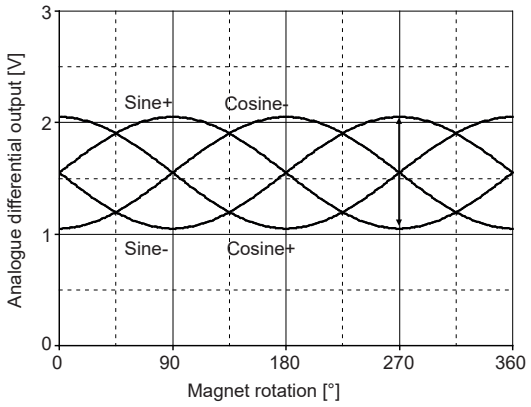


Fig. 9: Timing diagram for differential analogue output

Pin name	Pin function
“W/N_{Cos}”	Cosine negative
“V/P_{Sin}”	Sine positive
“U/N_{Sin}”	Sine negative
T_d/P_{Cos}	Cosine positive

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Amplitude	A	1	1.66	2.2	V	*
Amplitude difference	d_A		0	0.5	%	
Phase difference	d_{Ph}	89.8	90	90.2	°	
Sine offset	S_{offs}	–5	0	5	mV	
Cosine offset	C_{offs}	–5	0	5	mV	
Max. frequency	f_{Max}		1000		Hz	

* Amplitude = 1/2 of peak to peak value of the difference between the positive and negative signal.
The distance to the magnet and the temperature are within tolerances. To prevent saturation of the signals, the amplitude must never exceed 2.2 V.

AGC

Automatic gain control is enabled when the “AGCdis” parameter is set to 0. If the magnetic signal is changing the AGC is able to control the output signal amplitude in range between 0.8 V and 1 V. When the amplitude is less than 0.8 V, the gain is increased. When the amplitude is more than 1 V, the gain is decreased. The AGC gain has 16 levels and the range is from 0.5 to 2. Level 8 is at normal magnetic conditions.

Interpolator

When the magnet is rotated for 360° the sensors generates two perfect sinusoidal signals with phase difference of 90°. The interpolator is using those sinusoidal signals to calculate the current angle position and the angle position is output in various output formats. The calculation is performed in less than 1µs. The interpolation rates is selectable from 64 to 4096.

“Res” value	Interpolation rate	Resolution	Max. input freq.
0 0 0	4,096	0.0879°	500 Hz
0 0 1	2,048	0.1758°	1000 Hz
0 1 0	1,024	0.3516°	1000 Hz
0 1 1	512	0.7031°	1000 Hz
1 0 0	256	1.4062°	1000 Hz
1 0 1	128	2.8125°	1000 Hz
1 1 0	64	5.625°	1000 Hz
1 1 1	32	11.25°	1000 Hz

Zeroing

The output angle position data can be zeroed at any angle with resolution of 0.0879°. The relative output position is a difference between absolute position and data in zero register. The value in zero register can be changed by writing a desired value with TWI interface or with using a “Zero” input pin. With low to high transition of a signal on “Zero” pin the current absolute value is stored in zero register. When zeroing the relative position the chip must not be in power-save mode as the EEPROM is not accessible.

Incremental output

There are three signals for the incremental output: A, B and Ri. Signals A and B are quadrature signals, shifted by 90°, and signal Ri is a reference mark. The reference mark signal is produced once per revolution. The width of the Ri pulse is 1/4 of the quadrature signal period and it is synchronized with the A and B signals. The position of the reference mark is at zero.

The chart below shows the timing diagram of A, B and Ri signals with CW rotation of the magnet and positive counting direction. B leads A for CW rotation. The counting direction can be changed by programming the EEPROM with the “Sign” parameter.

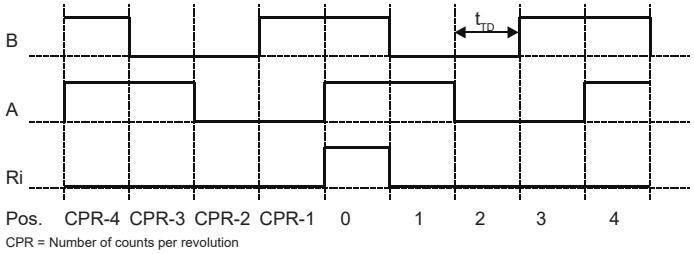


Fig. 10: Timing diagram for incremental output

The transition distance (t_{TD}) is the time between two output position changes. The transition distance time is limited by the interpolator and the limitation is dependent on the output resolution. The counter must be able to detect the minimum transition distance to avoid missing pulses.

Binary synchronous serial output SSI

Serial output data is available in up to 12 bit natural binary code through the SSI protocol. With positive counting direction and the CW magnet rotation, the value of the output data increases.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Clock period	t_{CL}	0.25		2 × tm	µs	
Clock high	t_{CHI}	0.1		tm	µs	
Clock low	t_{CLO}	0.1		tm	µs	
Monoflop time	t_m	15	19	25	µs	

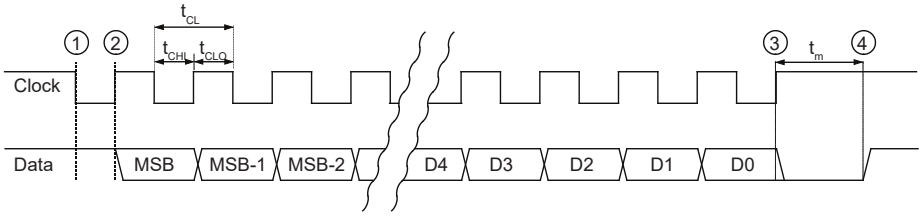


Fig. 11: SSI timing diagram with monoflop timeout

The controller interrogates the AM4096 for its positional value by sending a pulse train to the Clock input. The Clock signal must always start from high. The first high/low transition (point 1) stores the current position data in a parallel/serial converter and the monoflop is triggered. With each transition of Clock signal (high/low or low/high) the monoflop is retriggered. At the first low/high transition (point 2) the most significant bit (MSB) of the binary code is transmitted through the Data pin to the controller. At each subsequent low/high transition of the Clock the next bit is transmitted to the controller. While reading the data the t_{CHI} and t_{CLO} must be less than t_{mMin} to keep the monoflop set. After the least significant bit (LSB) is output (point 3) the Data goes to low. The controller must wait longer than t_{mMax} before it can read updated position data. At this point the monoflop time expires and the Data output goes to high (point 4).

SSIcfg	Descripion
0 0	No ring register operation
0 1	Ring register operation data length according to the resolution, data is not refreshed
1 0	No ring register operation
1 1	Ring register operation data length according to the resolution, data is refreshed

If the number of clocks is more than the data length than the behaviour of the SSI can be as defined with the SSIcfg parameter. If the “SSIcfg” parameter is set to 00 then the data is output only once (chart below).

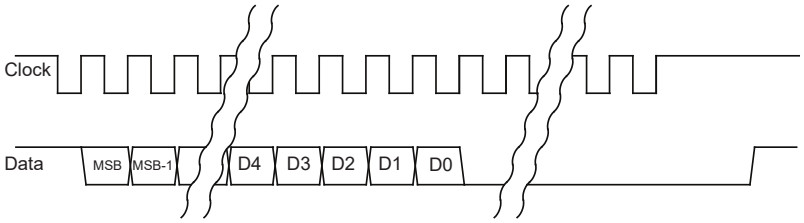


Fig. 12: SSI single read, SSIcfg is set to 00

To enlarge the reliability of reading the controller can read the same data more than once. The “SSIcfg” parameter must be set to “10” and the controller must continue sending the Clock pulses after the data is read without waiting for Tm (chart below). The same data will be output again and between the two outputs one logic zero will be output. The length of the data is depended of the resolution settings.

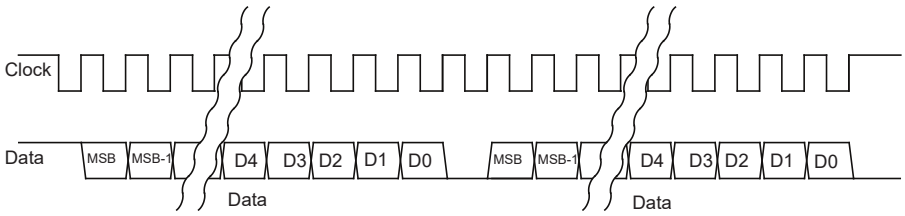


Fig. 13: SSI multi-read of the same position data, “SSIcfg” is set to 10

To speed-up the position reading of AM4096 the controller can constantly read the data. The “SSIcfg” parameter must be set to “11” and the controller must continue sending the Clock pulses after the data is read without waiting for Tm (chart below). Each data will be output as fresh position information and between the two outputs one logic zero will be output. The length of the data is depended of the resolution settings.

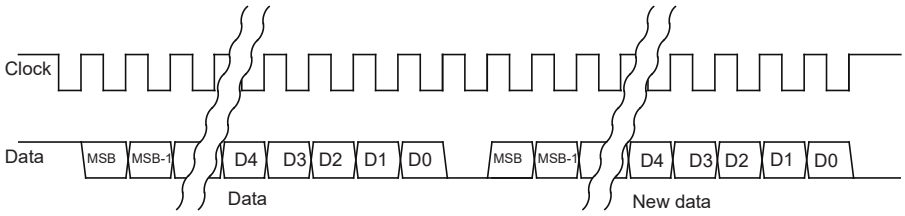


Fig. 14: SSI fast position read, SSIcfg is set to 11

Two wire interface (TWI) output

The output data can be read with the TWI interface which is described in the beginning of the data sheet. The available data are relative position, absolute position, magnet out of range and tacho output.

Data	Symbol	Adress	Position
Relative position	Rpos	32	<11:0>
Absolute position	Apos	33	<11:0>
Magnet too far	Weh	34	<14>
Magnet too close	Wel	34	<13>
Tacho overflow	Thof	35	<10>
Tacho out	Tho	35	<9:0>

Tacho output

The tacho output provides information of the current rotating speed. The rotating speed is calculated and output on the "V_{out}/T_{out}" pin when the "Dact" parameter is set to 1. The speed information is also available in the registers on address 35. The measuring range can be selected with the "Sth" parameter. The update time depends on the "Sth" parameter and selected resolution ("Res").

"Sth" value	Measuring range [Hz]	Measuring range [rpm]	Update time [ms]
0 0 0	2,048	122880	0.125 × 4096/Res
0 0 1	1,024	61440	0.25 × 4096/Res
0 1 0	512	30720	0.5 × 4096/Res
0 1 1	256	15360	1 × 4096/Res
1 0 0	128	7680	2 × 4096/Res
1 0 1	64	3840	4 × 4096/Res
1 1 0	32	1920	8 × 4096/Res
1 1 1	16	960	16 × 4096/Res

The "V_{out}/T_{out}" pin is an output from the 10 bit DA converter. The DA converter output voltage range is defined by the voltages on the "RefN" and "RefP" pins. See the linear voltage output description for detailed description of DA converter properties.

UVW output

UVW outputs can be output as digital signals when the "BufSel" parameter is set to 0. The number of pole pairs can be selected with "UVW" parameter. The number of signal periods (P) equals number of pole pairs. The timing diagram shows the signals when the position data is increasing. The U signal always starts at zero position regardless the signal period length. The resolution should be set to 4096 to ensure accurate transitions of the signals.

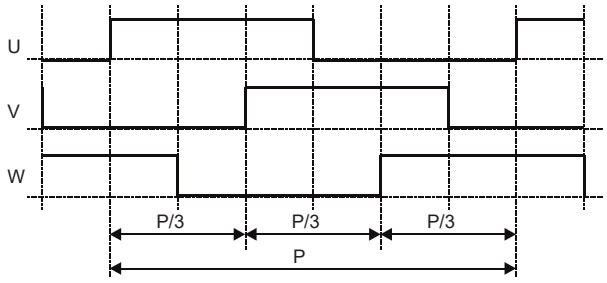


Fig. 15: UVW timing diagram for CW magnet rotation

"Uvw" value	Number of pole pairs	Signal period length [°]
0 0 0	1	360
0 0 1	2	180
0 1 0	3	120
0 1 1	4	90
1 0 0	5	72
1 0 1	6	60
1 1 0	7	51,4
1 1 1	8	45

Pin name	Pin function
"U/N_{Sin}"	U
"V/P_{Sin}"	V
"W/N_{Cos}"	W

Linear voltage output

The digital relative angular position information is converted into linear voltage with a 10 bit DA converter. The linear output voltage is a sawtooth shape and lies within thresholds defined with the two external pins RefP and RefN. The number of periods per revolution can be selected with the "Dac" parameter. The interpolator resolution setting should be more than 10 bit.

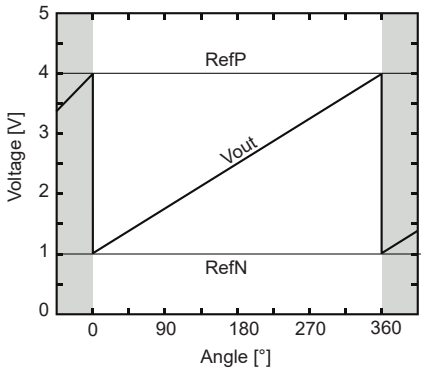


Fig. 16: One period per revolution ("Dac"= 0 0)

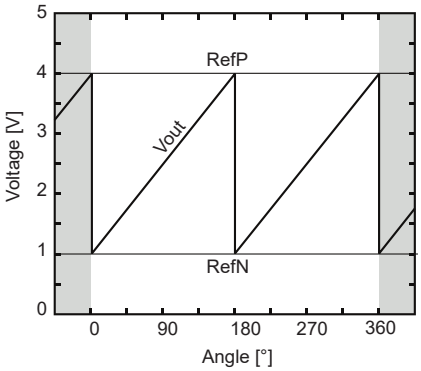


Fig. 17: Two periods per revolution ("Dac"= 0 1)

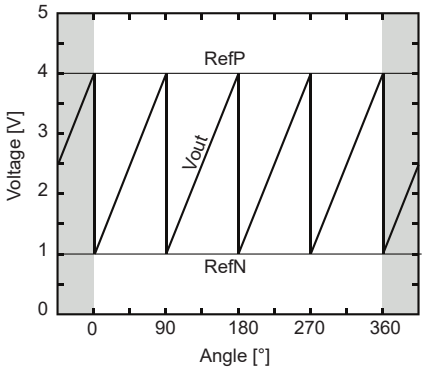


Fig. 18: Four periods per revolution ("Dac"= 1 0)

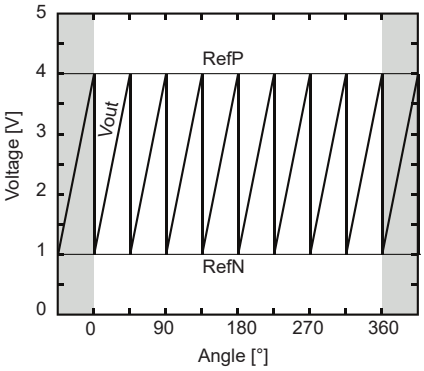


Fig. 19: Eight periods per revolution ("Dac"= 1 1)

Terminology:

RELATIVE ACCURACY: For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function.

OFFSET ERROR: This is a measure of the offset error of the DAC and the output amplifier. It is the difference between the output and the RefN voltage when the digital input value is 0. The units are in LSB.

GAIN ERROR: This is a measure of the span error of the DAC (including any error in the gain of the buffer amplifier). It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed in LSB.

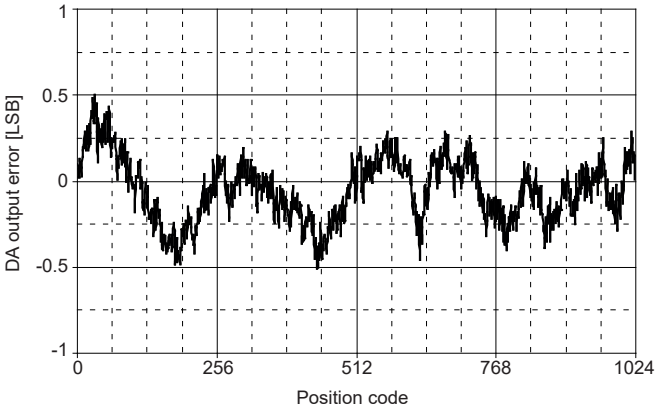


Fig. 20: Typical relative accuracy plot of the DAC

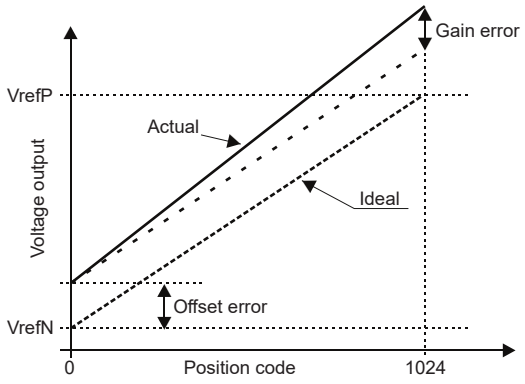


Fig. 21: Offset and Gain error of the DAC

DAC reference inputs characteristics:

Parameter	Min.	Typ.	Max.	Note
RefN internal pull down resistor		4.4 kΩ		
RefP internal pull up resistor		4.4 kΩ		
V_{RefN} input range	V_{ss}		Vext/2	
V_{RefP} input range	Vext/2		Vext	
V_{RefN} default value		7.4 % (Vext)		if RefN pin is not connected
V_{RefP} default value		92.7 % (Vext)		if RefP pin is not connected

DAC voltage output characteristics:

Parameter	Min.	Typ.	Max.	Note
Minimum output voltage		0 V		
Maximum output voltage		Vext-10 mV		Unloaded output
Output impedance		42 Ω		

DAC characteristics:

Parameter	Min.	Typ.	Max.	Units	Note
Resolution		10		bit	
Relative accuracy		±2		LSB	
Offset error		10		LSB	
Gain error		5		LSB	

Hysteresis

Hysteresis is the difference of the output position at the same magnet position when rotating direction is changed. Hysteresis can be separated into static and dynamic. Static hysteresis is independent of rotational speed, whilst dynamic hysteresis is directly related. The AM4096 uses an electrical and digital hysteresis (static) when converting analogue signals to digital. The hysteresis must always be larger than the peak noise to assure a stable digital output. Electrical hysteresis is set to 0.17°. Digital hysteresis can be set with the “Hist” parameter from 0 to 127 units. By default the digital hysteresis is set to 0. Each unit equals 360°/4096.

Dynamic hysteresis is caused by filter delay. Analogue signals are filtered with an RC filter (2 kΩ, 10 nF). The delay of such filter is 20 µs.

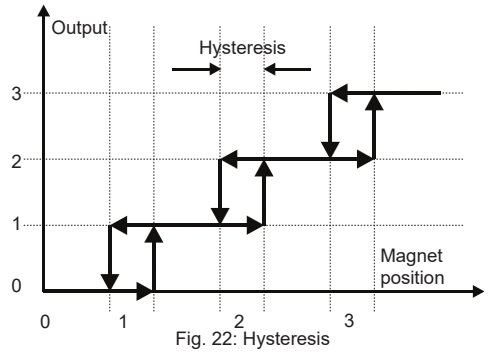


Fig. 22: Hysteresis

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Electrical hysteresis	$Hyst_e$	0.14	0.17	0.21	deg	*
Digital hysteresis	$Hyst_d$	0	0	11.16	deg	

* Measured at slow movement to avoid delay caused by filtering.

Nonlinearity

Nonlinearity is defined as the difference between the actual angular position of the magnet and the angular position output from the AM4096. There are different types of nonlinearity.

Differential nonlinearity is the difference between the measured position step and the ideal position step. The position step is the output position difference between any two neighbouring output positions, while the ideal position step is 360° divided by the resolution. Differential nonlinearity is mainly caused by noise. Differential nonlinearity is always less than one position step because there is a system that prevents missing codes. Chart on the left side shows a typical differential nonlinearity plot of the AM4096 with 12 bit resolution, 10 nF filtering and default parameters.

Integral nonlinearity is the total position error of the AM4096 output. Integral nonlinearity includes all position errors but does not include the quantisation error. Integral nonlinearity is minimised during production to better than ±0.2°. Chart on the right side shows a typical integral nonlinearity plot of the AM4096 with 12 bit resolution, a perfectly aligned magnet, 10 nF filtering and default parameters. Integral nonlinearity can increase if the default parameters are changed.

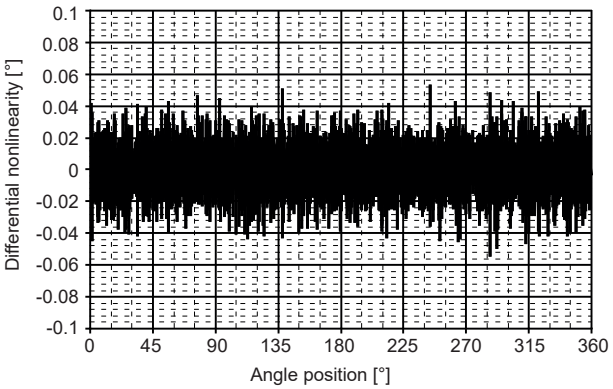


Fig. 23: Typical differential nonlinearity

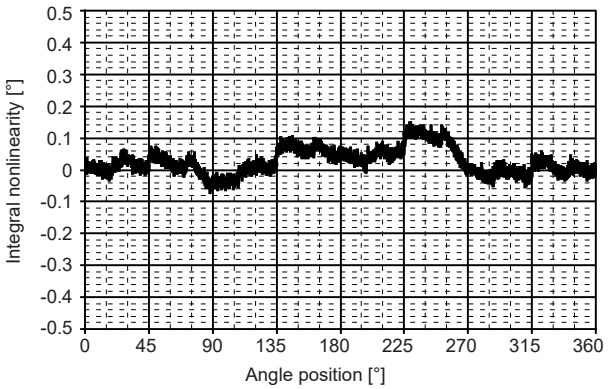


Fig. 24: Typical integral nonlinearity at optimal parameters

Power save mode

The AM4096 can operate in power save mode to minimise current consumption when position data update rate is not critical. Two types of power save mode are available, externally triggered and autonomous power save mode. It is recommended that when power save mode is used, the internal voltage regulator is not used and the voltage supply is 3.3 V.

Externally triggered power save mode can be done with “PSM” pin. While the “PSM” pin is high, the chip is operating in stand-by mode with no current consumption. When the “PSM” pin is switched to low the chip starts to operate normally and after 6ms the correct position data is available. When the position data is no longer needed, the chip can be put to sleep again.

Autonomous power save mode can be activated with “Pdie” parameter. If ”Pdie” is set to 1 then the chip starts to sleep with periodically 1ms wake-up time. The length of sleep time can be selected with “Pdtr” parameter.

“PSM” pin *	Operation	Note
Low	AM4096 operates normally	
High	AM4096 sleeps	**

* PSM pin is the only digital input that does not have internally pull-down resistor and it must not be left open.
** No communication with the chip is available.

“Pdie” value	Operation	Note
0	AM4096 operates normally	
1	AM4096 cyclically awakes according to the “Pdtr” parameter	*

* When autonomous power save mode is selected, the “PSM” pin should be low

“Pdtr” value	Active time	Inactive time	Units	Note
0 0	0.94	120	ms	
0 1	0.94	240	ms	
1 0	0.94	480	ms	
1 1	0.94	960	ms	

“Pdee” value	Available outputs	Note
0	All outputs are available	*
1	Only SSI and TWI outputs are available	**

* After PSM is switched from high to low it takes 6 ms before output information is usable.
** SSI and TWI data is available all the time. Position information is updated according to the “Pdtr” parameter.

Recommended magnet

The AM4096 can be supplied with a pre-selected magnet to ensure that optimum performance is achieved. Alternatively, magnets can be sourced from other suppliers but they must conform to the following guidelines.

To select a suitable magnet it is important to know the properties of the sensors. Hall Sensors are only sensitive to the perpendicular component of the magnetic flux density (B). The AM4096 has a Hall sensor array arranged in a circle with 1 mm radius. The sensors are located on the surface of the silicon. The nominal distance between the sensors and the magnet surface is 1.6 mm.

Magnets must be cylindrical in shape and diametrically polarized. The main criterion for magnet selection is the modulation of the perpendicular component of magnetic flux density at the location of the sensors (B_n) and a low offset of magnet modulation.

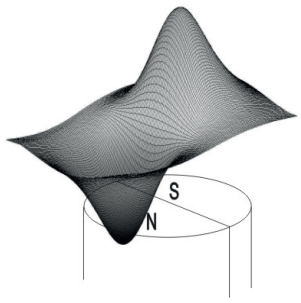


Fig. 25: Distribution of the perpendicular component of B

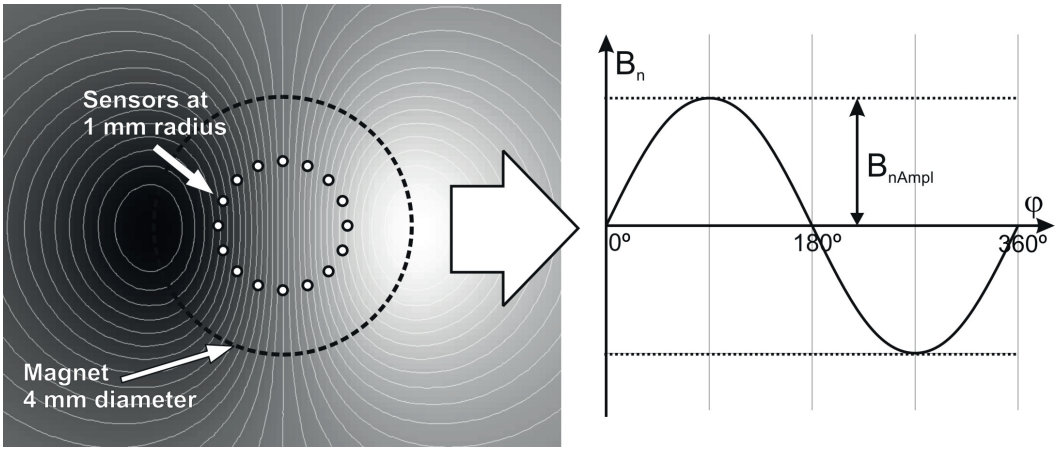


Fig. 26: Distribution of B_n and its modulation if the magnet is rotated through 360°

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Amplitude of B_n modulation	B_{nAmpl}		50		mT	*
Offset of B_n modulation	$B_{nOffset}$	–1		1	mT	**

* Typical value of B_{nAmpl} will give an analogue signal output with an amplitude of 0.68 V. The amplitude of the signal is proportional to the B_{nAmpl}: 1 Tesla equals 10,000 Gauss.
** Bad quality magnets offset the Bn modulation which results in increased integral nonlinearity when the magnet is not aligned correctly with respect to the chip.

We recommend that a magnet with the following parameters is used to provide the necessary modulation:

Parameter	Typ.	Unit	Note
Diameter	4	mm	
Length	4	mm	
Material	Sm2Co17		*
Material remanence	1.05	T	
Temperature coefficient	–0.03	% / °C	
Curie temperature	720	°C	

* Rare earth material magnets SmCo are recommended; however, NdFeB magnets can be used but they have different characteristics.

Magnet quality and the nonlinearity error

Each AM4096 is optimized during the production to give best performance with an ideal magnet when perfectly aligned.

An ideal magnet would have the polarization border exactly in the middle of the magnet. If the polarization is not exactly in the middle of the magnet then the modulation of the magnetic field has an offset.

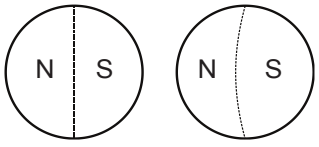


Fig. 27: Ideally polarized magnet and not ideally polarized magnet

The offset represents a mean value of Bn when the magnet is rotated through 360° and B_n is measured at 1.6 mm distance from the magnet surface and at 1 mm radius.

Offset will cause larger than normal integral nonlinearity errors if the sensors center placement is not in the center of the magnet rotation. Chart below shows an additional integral nonlinearity error caused by misalignment of the AM4096 for ideal and recommended magnets. Total integral nonlinearity is the summation of integral nonlinearity and the additional integral nonlinearity error caused by magnet displacement.

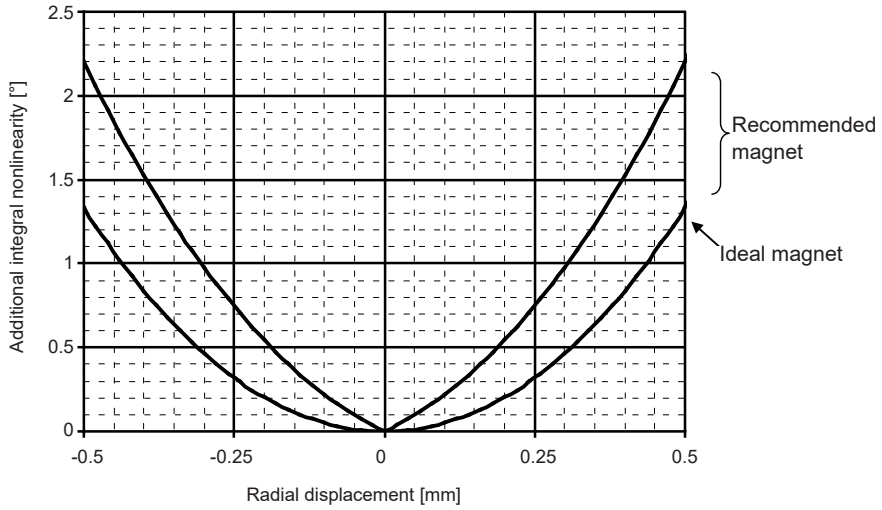


Fig. 28: Additional integral nonlinearity error caused by magnet displacement and quality

It is important that magnetic materials are not close to the magnet because they can increase the integral nonlinearity. They should ideally be at least 3 centimetres away from the chip. The magnet should be mounted in a non-magnetic carrier.

Magnet position

Magnet must be positioned above the AM4096 in the centre of hall sensor array. The centre of the sensor array is not in the centre of the AM4096.

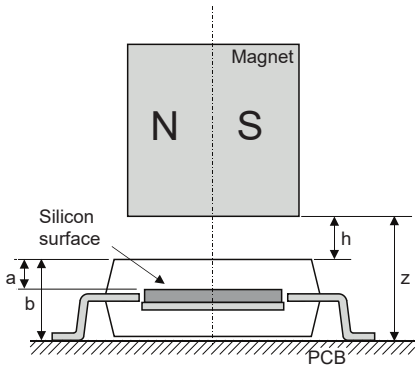


Fig. 29: AM4096 and the magnet with dimensions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Distance sensors – chip surface	a		0.75		mm	
Distance PCB plane– chip surface	b		1.86		mm	*
Distance chip surface – magnet	h	0.50	1.00	1.50	mm	
Distance PCB plane – magnet	z	2.36	2.86	3.36	mm	*

* For typical 40 µm copper thickness of PCB

Mounting instructions

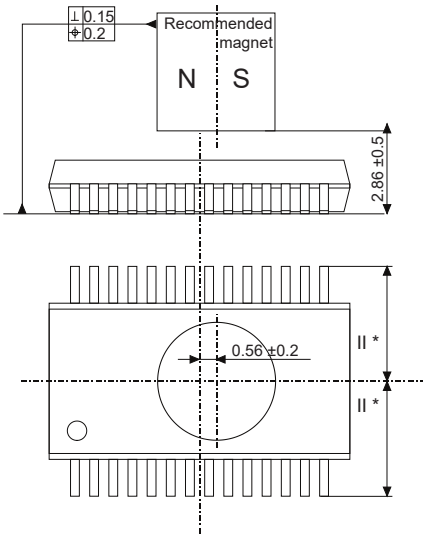


Fig. 30: Mounting instructions

Application scheme

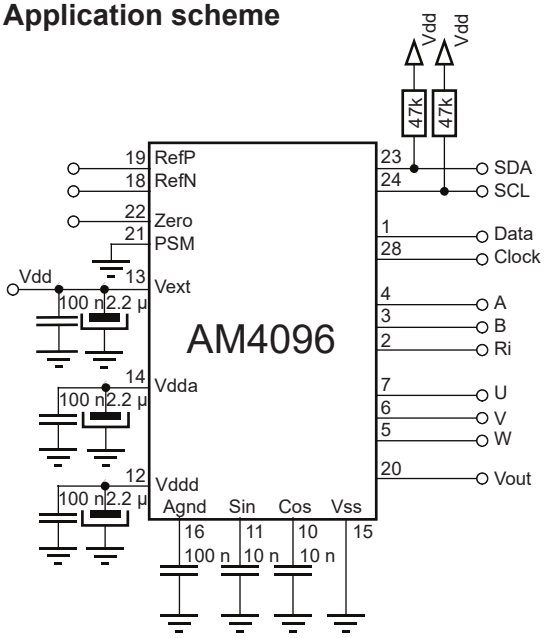


Fig. 31: Typical application scheme

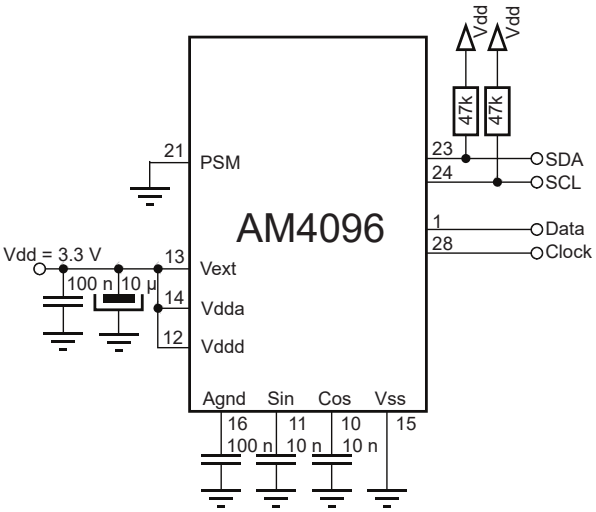


Fig. 32: Application scheme for autonomous power save mode

SSOP28 package dimensions

Dimensions:

Symbol	Min.	Typ.	Max.	Unit
A			2	mm
A1	0.05			mm
A2	1.65	1.75	1.85	mm
b	0.22		0.38	mm
c	0.09		0.25	mm
D	9.9	10.2	10.5	mm
E	7.4	7.8	8.2	mm
E1	5	5.3	5.6	mm
e		0.65		mm
K	0		10	deg
L	0.55	0.75	0.95	mm

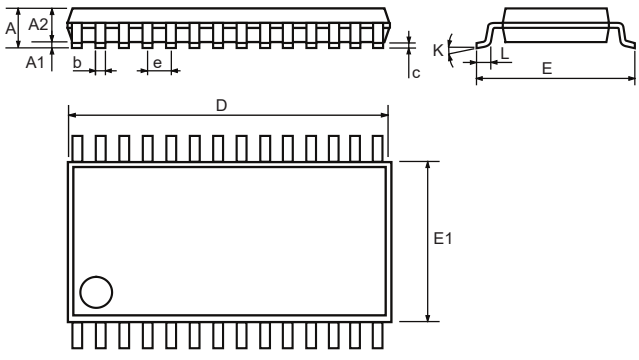


Fig. 33: Dimensional drawing

Ordering information

1. Angular magnetic Encoder IC

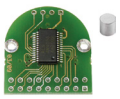
Part Number	Description
AM4096PT 	AM4096 Angular Magnetic Encoder IC with default functionality Output options: - SSI - Incremental - Linear voltage - UVW - TWI Programmable: - Differential buffered Sine/Cosine - Tacho SSOP28 plastic package Delivered in tubes (48 units per tube)

NOTE: Order quantity must be a multiple of 48 (one tube).
NOTE: Can be delivered in reels (special order)
NOTE: Magnet must be ordered separately! The Angular Magnetic Encoder IC part number does not include a magnet.

2. Magnet

Part Number	Description
RMM44A3C00 	Diametrically polarized magnet Dimensions: Ø4 mm × 4 mm

3. Sample Kits

Part Number	Description
RMK4 	AM4096 Angular Magnetic Encoder IC, on a PCB with all necessary components and a magnet, delivered in an antistatic box Output options: SSI, Incremental, Linear voltage, UVW, TWI Programmable: Differential buffered Sine/Cosine, Tacho

4. Interfaces

Part Number	Description
UPRGAM4096 	The UPRGAM4096 is a programming interface for use with AM4096 rotary magnetic encoder chip and RMK4 evaluation board. It connects simply to a computer via a USB port. The package includes USB 2.0 A-B mini cable and a ribbon cable with the appropriate connector for the RMK4 board

RMK4 sample kit

AM4096 on a PCB with all necessary components and a magnet, delivered in an antistatic box. RMK4 has all outputs available, by default it is configured for 5 V supply voltage and with 12 bit resolution.

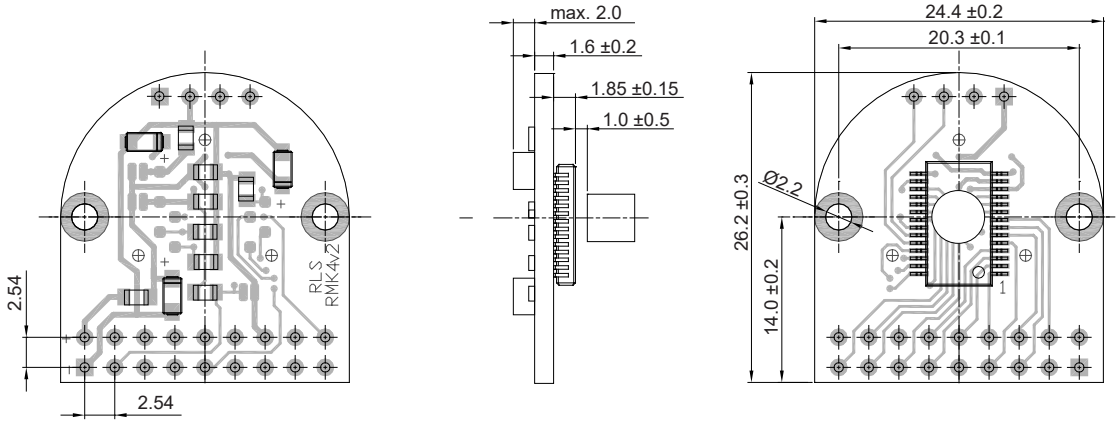


Fig. 34: RMK4 installation drawing

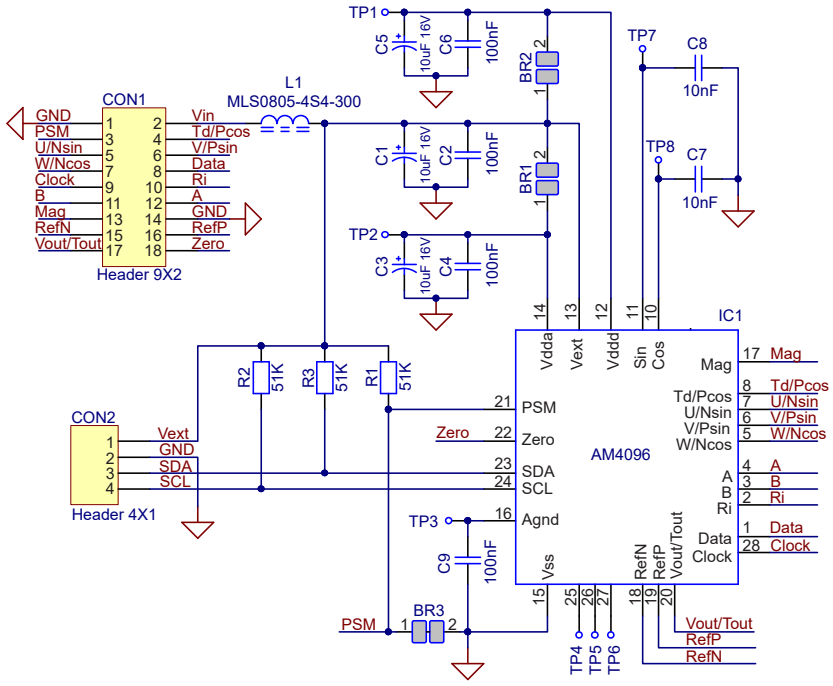
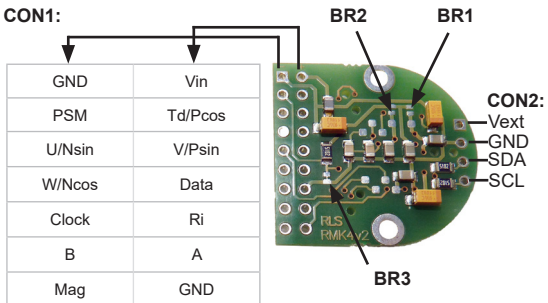


Fig. 35: RMK4 with schematic



GND	Vin
PSM	Td/Pcos
U/Nsin	V/Psin
W/Ncos	Data
Clock	Ri
B	A
Mag	GND
RefN	RefP
Vout/Tout	Zero

Bridge configuration:
BR1, BR2: Bridges for voltage regulators, opened by default.
BR3: PSM connection to Vss. To use PSM pin function, BR3 must be cut open. BR3 is closed by default.

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Document issues

Issue	Date	Page	Corrections made
1	19. 11. 2009	-	New document
2	10. 3. 2010	12	SSI data added
		22	UPRGAM4096 ordering information added
		23	New RMK4 image
3	4. 1. 2016	3	Moisture sensitivity level added
4	2. 6. 2016	19	SSOP28 package dimension added
5	23. 9. 2016	6	Time between EEPROM access amended
		21	RMK4 sample kit amended
6	18. 5. 2018	2, 3	Pin 9 amended
		6, 7	Monsel amended